Abstract—This brief presents a low-power fast-transient capacitor-less low-dropout regulator (CL-LDO) for system-on-a-chip applications. A low-quiescent-current class-AB amplifier with embedded slew-rate enhancement (SRE) circuit is proposed to improve both current efficiency and load transient performance. As the SRE circuit is directly controlled by the amplifier, only a minimum hardware overhead is required. The proposed CL-LDO is fabricated in a 0.18-µm standard CMOS process. It occupies an active area of 0.051 mm² and consumes a quiescent current of 10.2 µA. It is capable of delivering a maximum load current of 100 mA at 1.0-V output from a 1.2-V power supply. The measured results show that a settling time of 0.22 µs is achieved for load steps from 1 mA to 100 mA (and vice versa) with an edge time of 0.1 µs.

Index Terms—high slew-rate (SR), capacitor-less low-dropout regulator (CL-LDO), low-power, fast-transient.

I. INTRODUCTION

The low-dropout regulator is widely used to provide clean and ripple-free power supplies in battery-powered and portable applications. To enable fully integrated for system-on-a-chip, CL-LDOs have been widely researched [1]. The loop stability and load transient performance of CL-LDOs are regarded as the two most important design criteria due to the lack of a bulky output capacitor. To prolong the battery life, high power efficiency is required, which is indicated by a low quiescent current ($I_Q$) and low dropout voltage ($V_{DD}$). The main obstacle to load transient performance is the limited gate-voltage slew-rate (SR) of the pass transistor ($M_{PT}$). The SR is limited by the large gate capacitance of the $M_{PT}$ and the small slew current ($I_{SR}$) due to the low $I_Q$. Therefore, a low-power error amplifier (EA) with high-SR is desirable for the CL-LDO design.

In previous works, various strategies have been proposed for improving the current efficiency and load transient performance of CL-LDOs. The main approaches include designing low-power EAs with adaptive biasing techniques [3]-[6] and/or dynamic-operating SRE circuits [2]-[6], [8] to relieve the gate-voltage SR limitation. The adaptive biasing techniques increase $I_Q$ according to the load current ($I_{load}$), which improves the loop gain and unity-gain bandwidth (UGB) at heavy load conditions. Thus, better load (line) regulation and transient performances can be expected at the cost of higher power consumption. The SRE circuit is a vital part of CL-LDOs with a low $I_Q$ for load transient improvement, and it usually consists of sensing and driving circuits. The sensing circuit detects the load transient and generates control signals for the driving circuit, while the driving circuit is controlled to generate large extra currents only during transient response. Several techniques have been proposed to implement the sensing circuit, such as voltage-spike detector [2], [3], [6], capacitive coupling [4], current comparators [5], and high-pass filter [8]. However, the sensing circuit contributes to circuit complexity and requires extra area or current, which can be eliminated if the EA directly controls the driving circuit.

In this brief, a low-power CL-LDO with a high-SR class-AB amplifier is presented for improving both current efficiency and load transient performance. The conceptual scheme of the proposed CL-LDO is shown in Fig. 1. The SRE circuit consists of two driving circuits, one is embedded into the main linear regulation loop, and the other forms fast nonlinear feedback loops only for large transient steps. Hence, a dynamically boosted $I_{SR}$ is achieved with a minimum hardware overhead.

II. DESIGN OF THE PROPOSED CL-LDO

A. Circuit Design and Implementation

As shown in Fig. 1, $C_L$ stands for the parasitic capacitance of the load circuit. $C_L$ is a choosable capacitor for extending the maximum $C_L$ if necessary. $R_L$ represents the load circuit. The EA is a class-AB amplifier with complementary input pairs, a current-booster drive stage, and an embedded SRE circuit. Based on the compact two-stage cascode amplifier architecture in [10], the complementary input pairs are designed to obtain

![Diagram of the proposed CL-LDO](image-url)
class-AB operation for the drive stage instead of a floating class-AB control, and a current-mirror-based drive stage is applied after the summing circuit, as shown in Fig.2. In order to bias the two complementary input pairs that both work in the saturation region at low voltage supplies, nMOS level shifters are used for the pMOS input pair. The constant bias current $I_B$ is used to define the quiescent current of the summing circuit and drive stage for a constant total $I_Q$. Active $I_B$, such as current recycling [11], or adaptive $I_B$ can also be applied to enhance the performance but with tradeoffs among the power consumption, stability, and circuit complexity.

The SRE circuit is based on dynamic techniques and is implemented by using the source linear transistor (SLT) and drive stage. The DCT consists of $M_{DCDT_p}$ and $M_{DCT_n}$, which form fast nonlinear feedback loops to generate large extra charge (discharge) current $I_{chip}$ ($I_{ch}$) only in large transient steps when the DCT is turned on.

The size of $M_{PT}$ is $8,000\, \mu m/0.18\, \mu m$ for a maximum $I_{load}$ of 100 mA, as presented in Fig.2. For size reduction, the $M_{PT}$ is designed to operate in the triode region once $I_{load} \geq 80\, mA$ with a 1.2-V power supply since a nearly rail-to-rail gate-voltage swing is obtained. The other transistors are implemented as unit transistors in parallel for better device matching, except for the SLT and DCT. The design considerations of the SLT and DCT will be discussed later.

B. Stability Analysis

The small-signal modeling of the proposed CL-LDO is given in Fig.3, since the nonlinear feedback loop is only activated in transient steps. $C_{gdp}$ consists of $C_c$ and the gate-drain capacitor ($C_{gd}$) of $M_{PT}$. $C_{gsp}$ consists of the gate-source capacitor ($C_{gs}$) of $M_{PT}$ and the parasitic capacitor of EA. As current mirrors are used for the summing circuit and the drive stage, the poles inside of the EA are at high frequencies. Therefore, it is modeled as a one-pole system with transconductance $G_m$ and output impedance $R_{gate}$. The frequency response of the proposed CL-LDO is given in Equation (1), which is similar to the conventional one.

$$A_v(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{A_{dc}(1 - sC_{gdp}/g_{mpt})}{(1 + s/p_1)(1 + s/p_2)}$$

where the DC loop gain $A_{dc} = G_{m}R_{gate} \cdot g_{mpt}R_{out}$, and $R_{gate} \approx r_{ds,M17} \parallel r_{ds,M18}$, $R_{out} \approx r_{ds,MPT} \parallel R_L$.

$$p_1 = \frac{1}{[1 + g_{mpt}R_{out}]C_{gdp} + C_{gsp}R_{gate}}$$

$$p_2 \approx \frac{1 + g_{mpt}R_{out}C_{gsp} + C_{gsp}}{(C_LC_{gdp} + C_LC_{gsp} + C_{gdp}C_{gsp})R_{out}$$

$$UGB \approx A_{dc} \cdot p_1 \approx G_m/[C_{gdp} + C_{gsp}/(g_{mpt}R_{out})]$$

The dominant pole $p_1$ is located at the gate of $M_{PT}$, and the non-dominant pole $p_2$ is at the output node. Since $g_{mpt} \propto \sqrt{I_{load}}$ and $R_{out} \propto 1/I_{load}$, the $UGB \propto 1/\sqrt{I_{load}}$ and the $p_1, p_2 \propto 1/\sqrt{I_{load}}$. The CL-LDO might be unstable at certain small $I_{load}$ values. To keep a phase margin (PM) above 60°, the $p_2 \geq 2UGB$ should be ensured under all conditions.

Therefore, the maximum $C_L$ and minimum $g_{mpt}$ can be found as shown in Equation (3) by assuming $g_{mpt}R_{out} \gg 1$.

$$C_L \leq \frac{g_{mpt}}{2G_mC_{gdp} + C_{gsp}}C_{gdp}$$

$$g_{mpt} \geq \frac{C_L + C_{gsp}}{(C_{gdp} + C_{gsp})^2} \cdot 2G_m$$

A larger maximum $C_L$ can be obtained by a larger $C_{gdp}$, a smaller $G_m$, or a larger $g_{mpt}$. Whereas a larger $g_{mpt}$ requires...
a larger $I_{\text{load}}$, a smaller $G_m$ implies a smaller $I_{SR}$, and a larger $C_{gd}$ can be obtained by a larger $C_e$ at the penalty of UGB reduction. The worst case of loop stability happens at the minimum $I_{\text{load}}$ with the maximum $C_e$. A wide UGB is desirable for a fast response time; hence, $C_e$ should be minimized while keeping the linear regulation loop stable even at the worst case. In this work, the maximum $C_L$ of 100 pF is obtained at a minimum $I_{\text{load}} = 0.5 \text{ mA}$, $C_e = 0 \text{ pF}$, and a constant $I_Q$ of about 10 $\mu$A. Since a small $I_Q$ limits the transient performance, an embedded SRE circuit is developed to improve the transient performance while maintaining the constant low $I_Q$.

C. Design of the Embedded SRE Circuit

The basic drive stage is made up of current mirrors with ratio $\beta$, as shown on the left side of Fig.4. The gate current is

$$I_{SR0} = I_{op} - I_{on} = \beta (I_p - I_n) = \beta (g_{mp} + g_{mn}) \cdot \Delta V_{in}$$

(4)

where $g_{mp} (g_{mn})$ is the transconductance of the input pair $M_{1,2} (M_{3,4})$. $\Delta V_{in}$ is defined as $(V_{OUT} - V_{REF})$. The gains of the level shifters are neglected for simplicity. As shown in Fig.2, the $I_p$ and $I_n$ are given as follows:

$$I_p = I_B + I_a - I_d = I_B + g_{mp} \cdot \Delta V_{in}$$

$$I_n = I_B + I_c - I_d = I_B + g_{mn} \cdot \Delta V_{in}$$

(5)

From Equation (4), the $I_{SR0}$ is limited by the $\beta$, $g_{mp}$, and $g_{mn}$, namely by the small $I_Q$. Thus, a dynamic SRE circuit is desirable to improve the $I_{SR}$ for fast settling while maintaining the small $I_Q$ for high current efficiency and loop stability. The voltage-spike detector in [2]-[3], the APPSOS in [5], or the voltage damper in [8], can be added to the current mirrors in the drive stage or placed in parallel with the drive stage here. However, these SRE circuits require extra active area for the high-pass filter and/or extra current for the additional control circuits. As shown on the right side of Fig.4, the SRE circuit is developed and embedded into the EA in this work.

The SLT $M_{SLT_p} (M_{SLT_n})$ is biased into the deep triode region for a small steady-state drain-source voltage $V_{DS,SLT_p} (V_{DS,SLT_n})$, by sharing the bias voltage $V_{BP}$ ($V_{BN}$). The gate-source voltage $V_{GS,17}$ ($V_{GS,18}$) is the sum of the $V_{GS,15}$ ($V_{GS,16}$) and the $V_{DS,SLT_p}$ ($V_{DS,SLT_n}$). At the falling edge of $I_{\text{load}}$, any overshoot of $V_{OUT}$ will make $I_p$ increase from steady state. As a result, the $V_{DS,SLT_p}$ will increase dramatically because of triode operation; hence, the $V_{GS,17}$ will increase dramatically, as will the $I_p$. At the rising edge of $I_{\text{load}}$, any undershoot of $V_{OUT}$ will make $I_p$ decrease from steady state. The extent of decrease in the $V_{DS,SLT_p}$ is not significant due to the already small value at steady state; therefore, the $I_{op}$ will decrease mainly according to the $\beta$. A similar but contrary operation is found for the $V_{GS,16} (I_{on})$. Therefore, with properly designed SLT, the active value of $I_{op} (I_{on})$ can be significantly increased. The gate current becomes

$$I_{SR_s} \approx g_{m17} \cdot \frac{1 + g_{m15} \cdot \tau_{sp}}{g_{m15}} \cdot I_p - g_{m18} \cdot \frac{1 + g_{m16} \cdot \tau_{sn}}{g_{m16}} I_n$$

$$\approx \beta (1 + A_s) (g_{mp} + g_{mn}) \cdot \Delta V_{in}$$

(6)

where $g_{m17} \approx g_{m15} - g_{m18} \approx \beta g_{m16}$, and $A_s = g_{m15} \cdot \tau_{sp} = g_{m16} \cdot \tau_{sn}$ are assumed. $\tau_{sp} (\tau_{sn})$ is the linear resistance of $M_{SLT_p} (M_{SLT_n})$.

The $I_{SR_s}$ is enhanced by the gain $\beta$, which implies the enhanced $G_m$, $A_{dc}$, and UGB. However, a larger $G_m$ requires a larger minimum $I_{\text{load}}$ for stability. The size of SLT should be designed well for an optimal $A_s$. In this work, $A_s \approx 2$ is applied. With $\beta = 2$, the quiescent value of $I_{op} (I_{on})$ suffers from 1.5-µA increment. The same $I_Q = 10.2 \mu$A is used for a fair comparison; hence, $\beta = 4$ without SLT, as shown in Fig.5. With SLT, the settling time and undershoot are reduced by about 40%, from 0.49 $\mu$s/683 mV to 0.30 $\mu$s/380 mV. The response time is also improved because of the enhanced UGB and $I_{SR_s}$ with SLT.

For further improvement, the DCT $M_{DCT_p} (M_{DCT_n})$ is added to form the nonlinear feedback loop when large transient step happens. At such moment, large $I_{ch}$ ($I_{dch}$) is generated to quickly charge/discharge the gate capacitor of $M_{PF}$. The $M_{DCT_p} (M_{DCT_n})$ is directly controlled by the voltage $V_d$ ($V_b$) at node $d$ ($b$) of the folded cascode summing circuit. No additional sensing circuit is required, as the $V_d$ ($V_b$) is naturally sensitive to the transient response. The $M_{DCT_p} (M_{DCT_n})$ is in the cutoff region at steady state, and it will be turned on (off) automatically when $\Delta V_{OUT} > V_{trig} \ (\Delta V_{OUT} < V_{trig})$. The $V_{trig}$ is the trigger voltage of DCT, defined as the input variance that can turn on the DCT through the nonlinear feedback loop, as given in Equation (7).

$$V_{trig,p} \approx \left( \frac{V_{\text{th,M}_{DCT_p}} - V_{\text{off,M}_{DCT_p}}}{g_{mn} R_d} \right)$$

$$V_{trig,n} \approx \left( \frac{V_{\text{th,M}_{DCT_n}} - V_{\text{off,M}_{DCT_n}}}{g_{mp} R_d} \right)$$

(7)

where $R_d$ (of $b$) is the equivalent resistance of node $b$ ($d$).

Although $V_{trig}$ is controlled by the threshold voltage ($V_{\text{th}}$) of DCT, it is restrained by the gain of the nonlinear feedback loop. With properly designed $V_{BP}$ ($V_{BN}$) and transistors’ size, the $V_{th}$ variation has little effect on $V_{trig}$. A smaller $V_{trig}$ implies a smaller $\Delta V_{OUT}$. However, the $V_{trig}$ should be set properly to ensure the DCT is cutoff at steady state, even with some offsets at the input pairs. In this work, the $V_{trig}$ is set to around 100 mV, which is one-tenth of $V_{OUT}$. The
minimum length is used for the $M_{DCTp}$ ($M_{DCTn}$) to obtain small parasitic capacitances for a fast response time of the nonlinear feedback loop.

As shown in Fig.5, since the fast nonlinear feedback loop is formed when the DCT is turned on, the $\Delta V_{OUT}$ is significantly reduced to about 175 mV, as is the response time. As can be observed from the $I_{eh}$ ($I_{dch}$) waveform, the $M_{DCTp}$ ($M_{DCTn}$) is fully turned off before $V_{OUT}$ entirely recovers. Therefore, the nonlinear feedback loops do not disturb the stability of the CL-LDO. However, the hysteresis effect can affect the DCT to avoid the ringing behavior at the rising edge of $I_{load}$ and the overshoot-undershoot behavior at the falling edge. The hysteresis effect can be formed by either a hysteresis circuit, such as the current comparator in [5], or a short time delay that can be obtained by the inherent parasitic RC components of the layout process. In this work, the hysteresis effect is implemented via a parasitic RC delay to avoid the additional costs of using a hysteresis circuit. Once $\Delta V_{OUT} < V_{trig}$, $V_{OUT}$ recovers with $I_{SR}$ that is proportional to $\Delta V_{OUT}$. Since the DCT is turned off while $I_{load}$ is still rising, there might be a plateau period for $V_{OUT}$ when the settling of $V_{OUT}$ from the main linear regulation loop balances the load variation response of $V_{OUT}$. The finite bandwidth of the main linear regulation loop also limits the transient response.

The AC simulation results of the proposed CL-LDO are shown in Fig.6. With an estimated $C_L$ of 20 pF when fully integrated, a $PM > 60^\circ$ is achieved for an $I_{load}$ range from 0.5 mA to 100 mA, over process corners and temperatures. It is stable even at worst case ($I_{load} = 0.5 mA$ and $C_L = 100 \mu F$), though a small $PM$ occurs at FFF corners with high temperature. At heavy load conditions, when the $M_{PT}$ enters into the triode region and $R_{out}$ reduces dramatically, the gain of the power stage $g_{mpt} R_{out}$ is reduced, as is the $A_{dc}$ and $UGB$. The minimum $A_{dc}$ of 59.8 dB with a minimum $USB$ of 2.2 MHz is found at $I_{load} = 100 mA$.

### III. EXPERIMENTAL RESULTS

The proposed CL-LDO is fabricated using a 0.18-µm standard CMOS process. The chip micrograph with a shielding layer is presented in Fig.7, which shows an active area occupation of 0.031 mm². The input supply $V_{DD}$ is 1.2 V to 1.8 V, and $V_{OUT}$ is 0.8 V to 1.6 V with a minimum $V_{DD}$ of 200 mV. The measured line transient response is shown in Fig.8 with $V_{OUT} = 1.0 V$, $I_{load} = 1 mA$ and $C_L = 100 \mu F$. As $V_{DD}$ changes from 1.2 V to 1.8 V (and vice versa) within 5 µs, the $V_{OUT}$ suffers from a 6 mV variation. The measured load transient response is shown in Fig.9, where an off-chip load switch is used to generate the load steps. For the $I_{load}$ steps from 1 mA to 100 mA (and vice versa) within 0.1 µs, the settling time is 0.22 µs with an undershoot less than 200 mV. Due to the effects of the load switch and the effects of the parasitic components of the traces in measurement, the response time is a little longer than that in
simulation results. The measured load regulation is calculated as 8 mV/(100 − 1) mA, which is about 0.081 mV/mA.

The performance comparison with previously reported CL-LDOs is summarized in Table I. The figure-of-merit (FOM) in [2], FOM1, and in [3], FOM2, are adopted to evaluate the different current efficient CL-LDOs. The smaller FOM1 and FOM2 indicate the better performance in terms of the current efficiency and load transient response. Although the LDO in [6] achieves the best FOM1 as a larger CL is applied, this work achieves a FOM1 of 0.0206 V. Except for [3], which applies a longer edge time, this work achieves the smallest FOM2 of 0.0224 ns. When considering the effects of the minimum length (L) of transistors in different technologies, the FOM2 in [7] is adopted. This work achieves the smallest FOM2, which, together with FOM2 and FOM1, confirms the better performance regarding the current efficiency and load transient response.

IV. CONCLUSION

A low-power fast-transient CL-LDO employing a high-SR class-AB error amplifier is presented in this brief. The SRE circuit (SLT & DCT) is embedded into the amplifier with a minimum hardware overhead. The proposed CL-LDO is stable at a load current range from 0.5 mA to 100 mA with a maximum allowable CL of 100 pF and without any compensation. It occupies an active area of 0.031 mm² and consumes a quiescent current of 10.2 µA. A settling time of about 0.22 µs is measured when the load current steps from 1 mA to 100 mA (and vice versa) within 0.1 µs, and the undershoot is less than 200 mV.

Fig. 8. Measured line transient response of the proposed CL-LDO with an edge time of 5 µs, \( V_{\text{OUT}} = 1.0 \text{ V} \), \( I_{\text{load}} = 1 \text{ mA} \), CL = 100 pF.

Fig. 9. Measured load transient response of the proposed CL-LDO with an edge time of 0.1 µs, \( V_{\text{DD}} = 1.2 \text{ V} \), \( V_{\text{OUT}} = 1.0 \text{ V} \).

**REFERENCES**


