A 99-dB DR Fourth-Order Delta–Sigma Modulator for 20-kHz Bandwidth Sensor Applications

Youngkil Choi, *Student Member, IEEE*, Jeongjin Roh, *Member, IEEE*, Hyungdong Roh, *Student Member, IEEE*, Hyunseok Nam, *Student Member, IEEE*, and Songjun Lee

***Abstract*—A fourth-order single-bit delta–sigma modulator is presented for sensor applications. The loop filter is composed of both feedback and feedforward paths, and the modulator is implemented using fully differential switched-capacitor techniques. A test chip was fabricated in a 0.18-μm standard complementary metal–oxide semiconductor (CMOS) process. The chip core area is 1.22 mm^2, and its power consumption is 5.6 mW from a 3.0-V power supply. Measurement results show that a maximum 99-dB dynamic range is achievable at a clock rate of 3.2 MHz for the 20-kHz bandwidth. The designed chip is targeted for high-accuracy and wide-bandwidth sensor applications such as the resistor-based current sensors and the Hall-effect sensors in motor control systems.**

***Index Terms*—Analog-to-digital converter, delta–sigma modulator, high resolution, signal sensors, switched-capacitor circuit.**

I. Introduction

DELTA–SIGMA modulators with high resolution are widely used in the areas of medical instrumentation, acoustic sensor applications, distributed sensor applications such as seismic detections for oil exploration, and digital audio equipment such as DVD recording systems [1]–[3]. The sensors used in these various applications have different bandwidths from near dc to several tens of kilohertz. For example, temperature sensors have a bandwidth that usually does not exceed 100 Hz; however, typical linear Hall-effect sensors have a bandwidth of up to 25 kHz [4]. In addition, high-accuracy sensors with more than 85-dB signal-to-noise-plus-distortion ratio (SNDR) within 20-kHz bandwidth are required for the accurate current sensing in the motor control market [5], [6]. Fig. 1 shows a typical block diagram of motor control systems. The most common technique for current measurements in motor control is to use the shunt resistors. The voltage drop across the resistor is digitized by the delta–sigma modulator. The Hall-effect sensors are used in high-current applications, where the power loss with the shunt resistor becomes significant [6]. Table I shows our modulator specification required for these high-accuracy and wide-bandwidth sensors of 20-kHz bandwidth.

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The authors are with the Department of Electrical and Computer Engineering, Hanyang University, Ansan 426-791, Korea (e-mail: jroh@hanyang.ac.kr).

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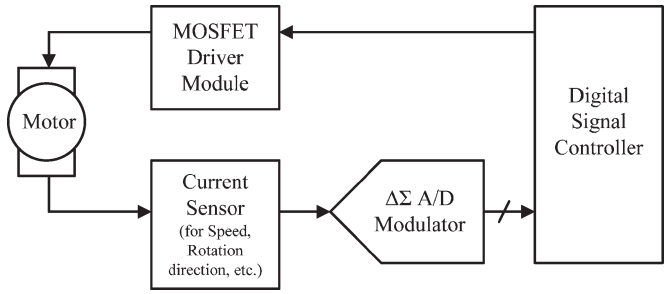

Fig. 1. Block diagram of motor control systems.

TABLE I
MODULATOR SPECIFICATION

Parameter	Value
Signal bandwidth	20 kHz
Sampling frequency	3.2 MHz
SNDR	> 85 dB
Power supply voltage	3 V
Power consumption	less than a few mW

Several different modulator architectures have been used to achieve high resolution. As listed in Table II, each type of architecture has advantages and disadvantages [7]. Among the modulator architectures, the high-order single-loop architecture is highly attractive whenever a high signal-to-noise ratio (SNR) and simple circuit design are important. Several topologies have been successfully used in delta–sigma modulator design. One interesting topology that has been used is the distributed feedforward (DFF) architecture, presented in [8] and [9]. The advantage of this topology is that the loop filter does not process the input signal, and hence, the configuration allows for the use of more efficient operational amplifier (opamp) architectures. Another topology uses distributed feedback (DFB). The feedback signals in this topology are fed to each integrator input terminal with different weight factors; detailed explanations are presented in [7] and [10]. The main advantage of this topology is that it is easy to implement, with low sensitivity to component variations. A drawback of this topology is that the integrator outputs contain significant amounts of the input signal and filtered quantization noise [7]. DFB circuits thus tend to be larger and more power hungry than DFF circuits. As mentioned above, it is important to note that the selection of the modulator architecture is related to the chip area, opamp requirement, and power consumption. As stated in [11], for small sensor arrays

TABLE II
COMPARISON OF MODULATOR ARCHITECTURES

Modulator type	SNR vs. OSR ratio	Idle-tons / Linearity	Circuit design simplicity	Stability issues
Low-order single-loop single-bit	×	×	O	O
High-order single-loop single-bit	O	O	O	×
Multi-loop cascade	O	×	×	O
Multibit	O	×	×	O

and single-chip combinations of multiple sensor interfaces used in underwater acoustic sensor networks, the single-loop single-bit architecture is the most popular choice among various delta–sigma modulator architectures. For one thing, high accuracy can be obtained without imposing severe matching requirements for the circuitry. Therefore, in this paper, the modulator architecture selected for sensor applications is a single-loop single-bit delta–sigma modulator, and the modulator has a mixed loop topology with both feedback and feedforward paths. This enables the modulator to combine the advantages of both DFF and DFB topologies. No active summing circuit based on opamp is required; thus, only four opamps are necessary, as would be the case in a DFB architecture.

Following the introduction, the next section of this paper discusses how to make decisions concerning some specifications using classical equations and shows the results obtained through behavioral simulations. Section III relates the implementation of the detailed blocks of our modulator, as well as a transistor-level simulation using HSPICE. Section IV describes the test setup used to achieve the experimental results. We provide the figure of merit (FOM) of the designed modulator as compared with other state-of-the-art modulators. Finally, the conclusions of this paper are given in Section V.

II. MODULATOR SYSTEM-LEVEL DESIGN

It is necessary to make several decisions about the detailed specifications of a delta–sigma modulator after selecting the modulator's architecture. There is some degree of freedom that exists in the design of the delta–sigma modulator for a given dynamic range (DR). These consist of the oversampling ratio (OSR), the loop order (n), and the quantizer resolution (B). The DR of the modulator is defined as the ratio of the power in a full-scale input to the power of a sinusoidal input for which the SNR is one (0 dB). The DR is related to OSR, n, and B, according to [10]

$$\mathrm{DR} = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right)\mathrm{OSR}^{2n+1}(2^B-1)^2. \tag{1}$$

Because the architecture used for the modulator is a single-bit one, B in (1) is 1. For the case of a single-bit architecture, the relationship becomes

$$\mathrm{DR} = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right)\mathrm{OSR}^{2n+1}. \tag{2}$$

To achieve a DR of 100 dB, we have to choose a proper n and OSR. Most of the high-resolution delta–sigma modulators for sensor applications have an OSR from 64 to 128. We chose $\mathrm{OSR} = 80$ and substituted (2) with different loop orders. For example, at $n = 3$, the theoretical DR is 113.6 dB. In the case of $n = 4$, the DR is 142.8 dB. This is the maximum attainable DR corresponding to the ideal case without considering stability. Real implementations will result in degradation in the achievable DR, with a detailed analysis found in [7]. Furthermore, the DR should be 10–20 dB more than the desired DR to allow for the inevitable DR degradation brought about due to circuit nonidealities. Thus, the loop order of $n = 3$ was discarded, and the single-bit single-loop delta–sigma modulator with an $\mathrm{OSR} = 80$ and $n = 4$ was chosen.

The DR is not only determined by the systematic factors mentioned above but limited by kT/C noise as well, since the noise level in the signal band is determined by the white kT/C noise, as discussed in [7]. The first integrator is the one most responsible for the overall performance in single-loop modulators. The DR of a delta–sigma modulator, where the resolution is limited by the kT/C noise of the first switched-capacitor integrator stage, is given by [10]

$$\mathrm{DR} = \frac{S_S}{S_{kT/C}} = \frac{(V_{SW})^2 \times \mathrm{OSR} \times C_S}{8kT}. \tag{3}$$

In the above equation, S_S and $S_{kT/C}$ are the power of a full-scale sinusoidal input and the power of the kT/C noise, respectively. V_{SW} is the amplitude of a full-scale sinusoidal input to the modulator and is set to 3 V in this paper. k is the Boltzmann's constant, T is the absolute temperature, and C_S is the sampling capacitance of the first integrator. To achieve the 110-dB DR in (3), the sampling capacitance should be 4.6 pF, but we used 5 pF as the sampling capacitance, taking some margin into consideration.

A block diagram of a single-bit fourth-order delta–sigma modulator is given in Fig. 2, in which X, Y, and E are an

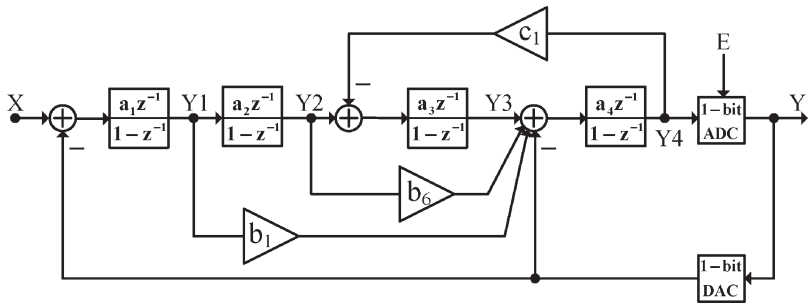

Fig. 2. Single-bit fourth-order delta–sigma modulator block diagram [12].

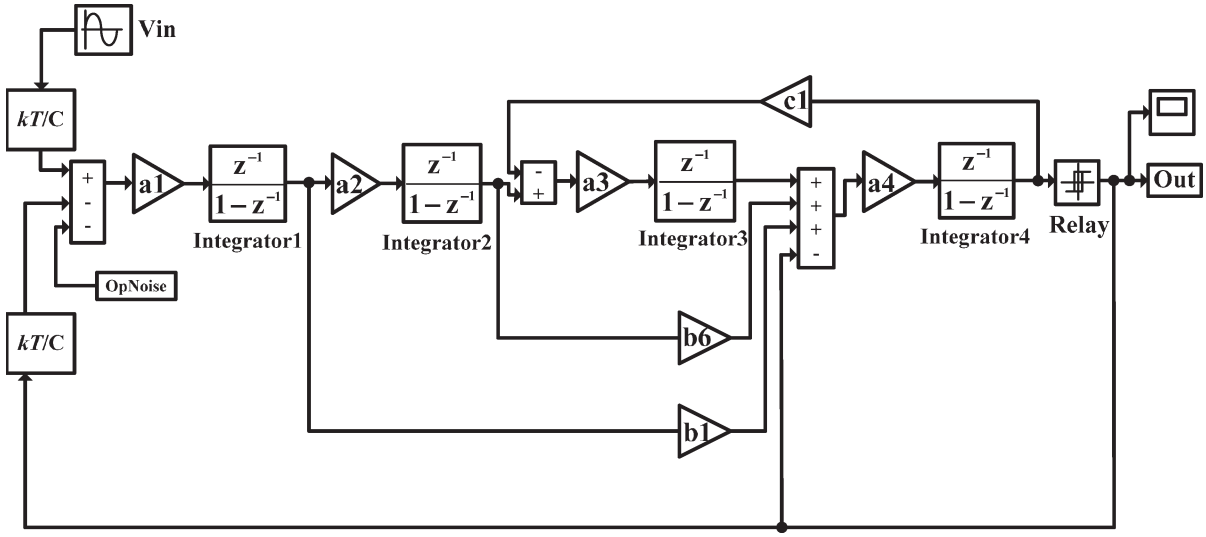

Fig. 3. SIMULINK model of the modulator.

input, an output, and a quantization error, respectively. The outputs of the first integrator and the second integrator are connected to the input of the fourth integrator through the feedforward paths. The feedforward factors are b_1 and b_6. The feedback around the last two integrators forms a local resonator. By choosing the appropriate feedback factor c_1, the complex zeros can be located to give optimum noise suppression in the signal band.

By the feedback system analysis [7], the output of the delta–sigma modulator can be given by

$$Y(z) = \text{STF}(z) \cdot X(z) + \text{NTF}(z) \cdot E(z) \tag{4}$$

where STF(z) and NTF(z) mean the signal transfer function and the noise transfer function, respectively. The transfer functions of the designed modulator can be expressed as given in (5) and (6), shown at the bottom of the page.

In this design, the maximum gain of the NTF is set to approximately 1.5 to guarantee the stability of the modulator [7], [12]. Furthermore, we evaluated the stability of this chip through extensive simulations since instability occurs when the amplitude or the frequency of the input signal exceeds a specific value. The loop coefficients in Figs. 2 and 3 are determined from the NTF as follows:

$$a_1 = \frac{1}{3}, \quad a_2 = \frac{3}{25}, \quad a_3 = \frac{1}{10}, \quad a_4 = \frac{1}{10}$$
$$b_1 = \frac{6}{5}, \quad b_6 = 1, \quad c_1 = \frac{1}{6}.$$

Table III lists each capacitance according to the above coefficients, which is shown in detail in Fig. 7. In addition, three kinds of unit capacitors are used to implement this modulator, considering the chip area and common-centroid structure. The capacitors of the first integrator use a 250-fF unit capacitor. All other capacitors except for C_{b1} are made up of 100-fF unit

$$\text{STF}(z) = \frac{a_1a_4b_1z^2+(a_1a_2a_4b_6-2a_1a_4b_1)z+(a_1a_2a_3a_4-a_1a_2a_4b_6+a_1a_4b_1)}{z^4+(a_4-4)z^3+(6+a_3a_4c_1-3a_4)z^2+(a_1a_4b_1+a_1a_2a_4b_6+3a-2a_3a_4c_1-4)z+(a_3a_4c_1+a_1a_2a_3a_4-a_1a_2a_4b_6-a_1a_4b_1-a_4+1)} \tag{5}$$

$$\text{NTF}(z) = \frac{z^4-4z^3+(6+a_3a_4c_1)z^2-(4+2a_3a_4c_1)z+a_3a_4c_1+1}{z^4+(a_4-4)z^3+(6+a_3a_4c_1-3a_4)z^2+(a_1a_4b_1+a_1a_2a_4b_6+3a-2a_3a_4c_1-4)z+(a_3a_4c_1+a_1a_2a_3a_4-a_1a_2a_4b_6-a_1a_4b_1-a_4+1)} \tag{6}$$

TABLE III
CAPACITANCES

Capacitor	Integrator1	Integrator2	Integrator3	Integrator4
C_S	5.00 pF	0.30 pF	0.60 pF	0.20 pF
C_I	15.00 pF	2.50 pF	6.00 pF	2.00 pF
C_{b1}				0.24 pF
C_{b6}				0.20 pF
C_{c1}			0.10 pF	
C_{unit_cap}	250fF	100fF (except for C_{b1})		
		120fF (only for C_{b1})		

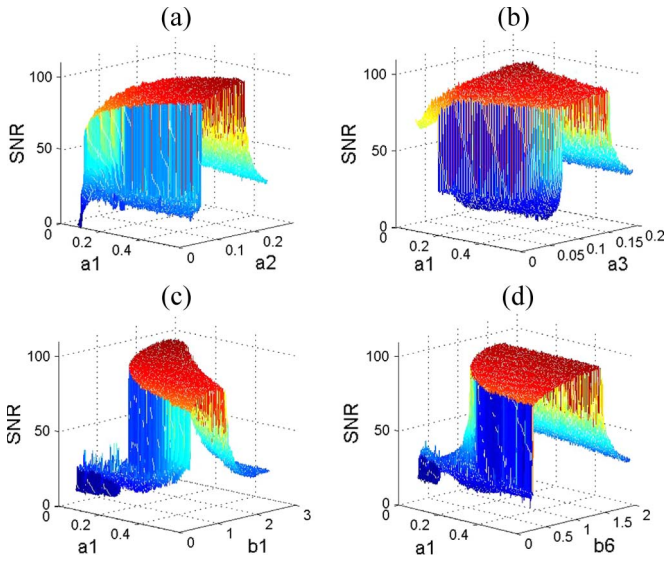

Fig. 4. SNR versus loop coefficients' variation.

capacitors. Fig. 3 is a SIMULINK model used to perform the behavioral simulation of the single-bit fourth-order delta–sigma modulator.

Fig. 4 shows 3-D plots of the SNR as a function of the loop coefficient a_1 and one other. Since the first integrator gain a_1 is more significant, we show the SNR variation with a_1 and another one to show the output in a 3-D plot. We have also performed other possible combinations of coefficient variations. These are performed using SIMULINK, and we show the results of extensive SNR simulations. In Fig. 4, we observe that increasing the loop coefficients will slightly increase the performance of the modulator but can lead to instability if the coefficients are increased too much. Therefore, we chose the suitable loop coefficients as previously mentioned for stable operation.

There are basically four types of models in Fig. 3: 1) the kT/C noise model, 2) the OpNoise model, 3) an integrator model with nonidealities, and 4) a quantizer model. Of these, the kT/C noise model may seriously affect the performance of the modulator. The kT/C noise model represents the switch thermal noise, which is limited by the time constant of the switched capacitors or the bandwidth of the opamp. The kT/C noise power e_T^2 is written as [13], [14]

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_S)^2}df = \frac{kT}{C_S} \tag{7}$$

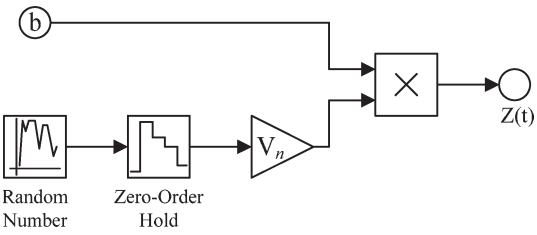

Fig. 5. Operational amplifier noise model (OpNoise block) [9].

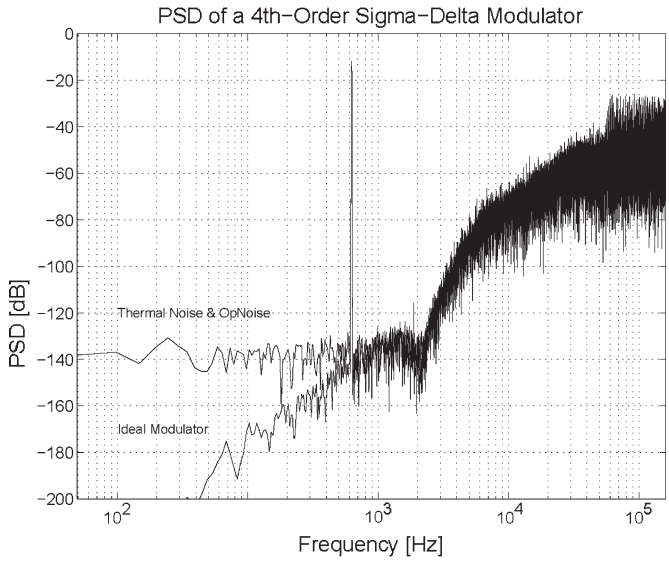

Fig. 6. PSDs of single-bit fourth-order delta–sigma modulator output with and without the thermal noise and opamp noise model.

where R_{on} is a finite resistance.

Another model is the OpNoise model, which is used to simulate the effect of the opamp noise. Fig. 5 shows a detailed representation of the OpNoise block in Fig. 3. Here, V_n signifies the total rms noise voltage of the opamp referred to the integrator input. The integrator model is implemented as a real integrator model with nonidealities (such as finite gain, bandwidth, slew rate, and saturation voltages). Following the fourth integrator is a quantizer block that includes some nonidealities (such as the offset or the hysteresis). The quantizer model was created using a simple relay model [14].

It is important to evaluate how sensitive the modulator is to the nonidealities mentioned above. To determine this, we first implemented the ideal modulator using SIMULINK models. Then, we added the blocks representing the nonidealities to the ideal modulator in turn. To optimize the modulator performance limited by the nonidealities, we attempted to simulate the modulator with the nonidealities several times; we estimated the power spectral densities (PSDs) of the modulator output bitstream obtained by changing the values of the nonidealities. The PSDs of the modulator output bitstream obtained in the simulation with and without the nonidealities are shown in Fig. 6. In the case of the ideal modulator, the SNDR obtained with an input signal of -4 dB is 99.2 dB. In the case of the modulator with nonidealities, the SNDR obtained with an input signal of -4 dB is 96.2 dB. Each spectrum is obtained with a fast Fourier transform on 65 536 samples with a Hanning window.

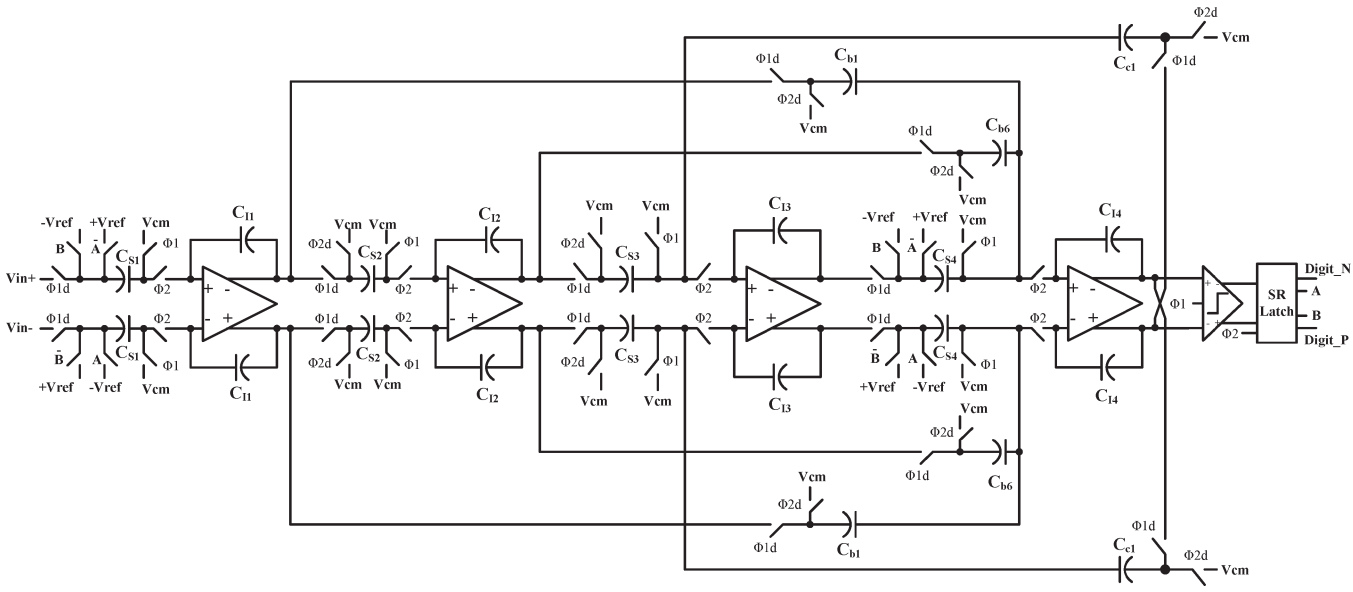

Fig. 7. Single-bit fourth-order delta–sigma modulator.

III. Circuit Design

A. Switched-Capacitor Integrator

The proposed delta–sigma modulator is implemented using a fully differential switched-capacitor technique. A fully differential topology has basically two advantages: 1) a higher immunity to environmental noise and 2) a wider DR. The modulator in Fig. 7 is controlled by two-phase nonoverlapping clocks: $\Phi 1$ for the sampling phase and $\Phi 2$ for the integration phase. Delayed clocks of the two phases ($\Phi 1d$ and $\Phi 2d$) are used to reduce the effects of charge injection in the switched-capacitor circuits. The input signal is sampled from the sampling capacitance during $\Phi 1$. During $\Phi 2$, the charge transfer takes place from the sampling capacitance to the integration capacitance to perform the integration function.

The modulator consists of four noninverting delaying integrators to avoid the double-settling problem. In Fig. 7, both the first and fourth integrators use two symmetrical reference voltages, positive ($+Vref$) and negative ($-Vref$), which are equal to the supply voltages (3 and 0 V). This is because lowering the feedback levels reduces the DR of the converter. The switches in this design were implemented using transmission gates, negative-channel MOS (NMOS) transistors, and positive-channel MOS (PMOS) transistors. The NMOS and PMOS transistors were appropriately sized to keep their on-resistance low enough to limit harmonic distortion. In our modulator, there is no need to use any clock bootstrapping circuit to boost the driving voltage, since the supply voltage is sufficiently high.

B. Opamps

Although all analog components are important, the most critical circuit in determining the settling speed and noise performance of the integrator is the opamp [15]. Fig. 8 shows the schematic of a fully differential folded-cascode opamp with switched-capacitor common-mode feedback (SCCMFB). The SCCMFB is based on the use of switched capacitors and has an advantage in power reduction, because no static current is consumed to generate the midpoint of the differential swing.

The important specifications for the design of an opamp are 1) open-loop dc gain, 2) unity-gain frequency ($F_{\rm u}$), 3) phase margin (PM), 4) slew rate, and 5) output swing. A general rule of thumb is that the sampling frequency ($F_{\rm s}$) should be at least five times lower in frequency than the $F_{\rm u}$ of the opamp, assuming that little slew-rate behavior occurs and the PM is greater than 70°. In our design, we used two versions of the opamp, which consumed different currents. Opamp1 denotes the opamp used in the first integrator, and opamp2 indicates the opamp used with the rest of the integrators. Fig. 9 shows the simulated ac response of opamp1 when driving a 6-pF effective load capacitance (C_{L-eff}) [16]. The open-loop dc gain of opamp1 is 73 dB, with an $F_{\rm u}$ of 54 MHz and a PM of 87.7°. Fig. 10 shows the simulated ac response of opamp2, the version used in the other integrators, when driving a 2-pF C_{L-eff}. For the second opamp version, the total quiescent currents are reduced by a factor of four. Table IV shows the simulated results of opamps obtained using the HSPICE tool.

In addition to the thermal noise mentioned in Section II, flicker noise in MOS transistors can result in a serious noise component when referring to the opamp input. Flicker noise is also called $1/f$ noise because it has a spectral density that varies approximately inversely with the frequency. The PSD of $1/f$ noise is given by the following equation [7]:

$$S_{\frac{1}{f}}(f) = \frac{K}{WLC_{ox}f}(\mathrm{V}^2/\mathrm{Hz}) \tag{8}$$

where W and L are the width and length of the transistor, C_{ox} is the gate capacitance per unit area, and f is the frequency. Here, K is a process-dependent constant on the order of 10^{-25} $\mathrm{V}^2\mathrm{F}$. The input-referred $1/f$ noise of a delta–sigma modulator is dominated by the input-referred $1/f$ noise of the opamp in the first integrator. Because of noise shaping, the opamp

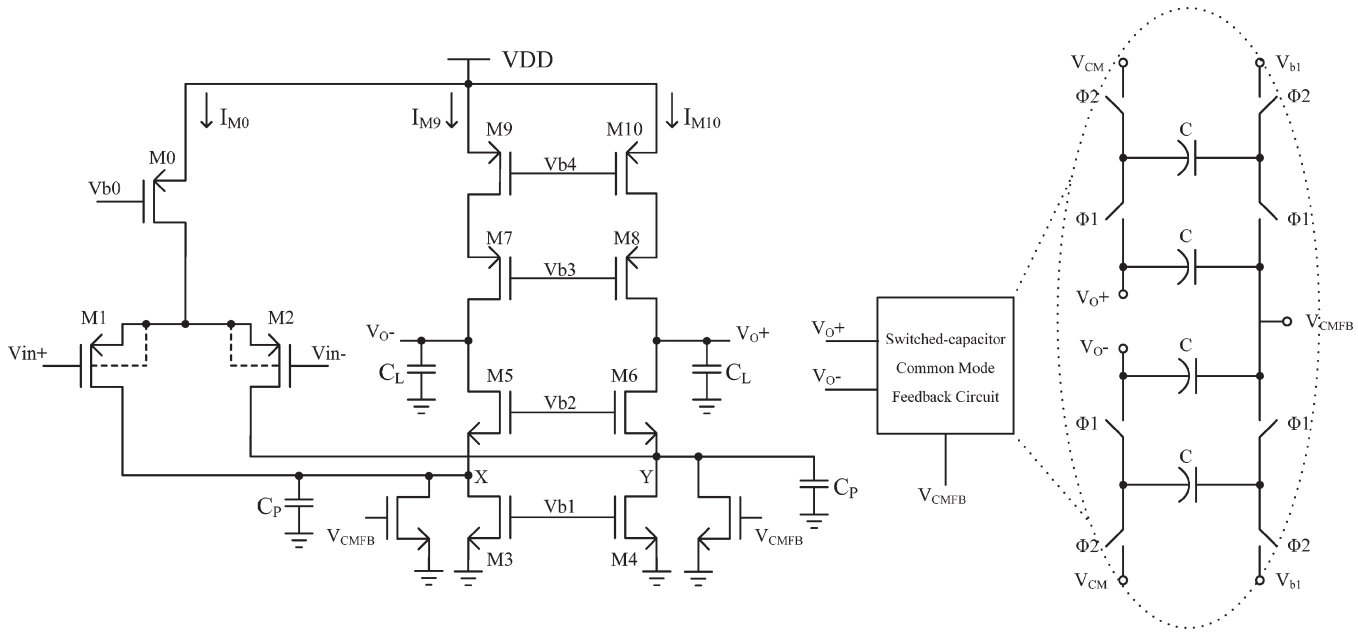

Fig. 8. Fully differential folded-cascode opamp.

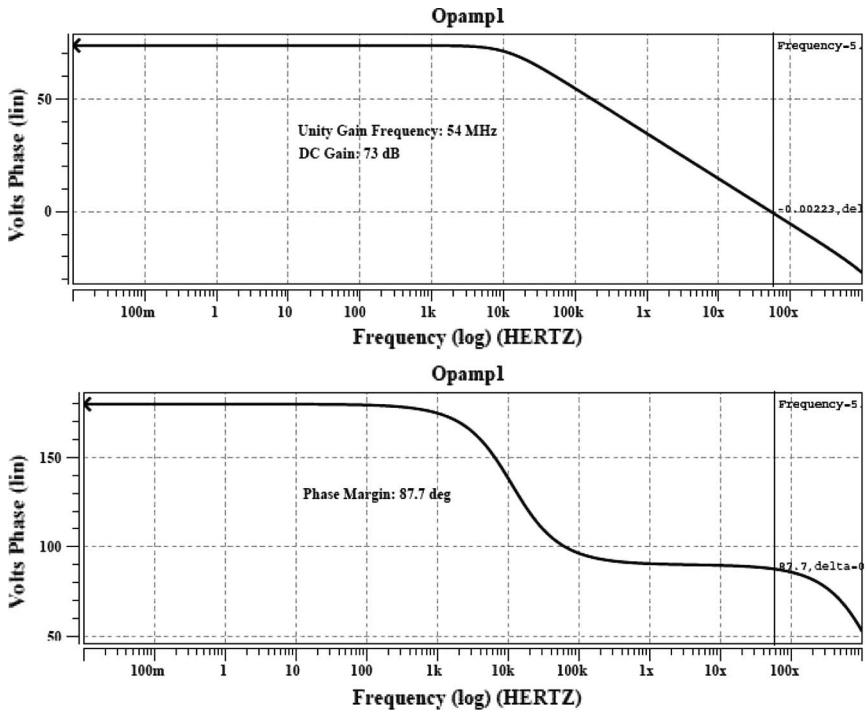

Fig. 9. AC simulation wave of Opamp1.

contributions in succeeding integrators to the overall $1/f$ noise of the delta–sigma modulator can be neglected [7]. There are several techniques used to minimize the effect of $1/f$ noise. A common technique is to increase the size of input transistors at the input stage. As discussed above, $1/f$ noise is dependent on the reciprocal of $W \times L$. The input transistor sizes for opamps are summarized in Table V. A more detailed description of this technique is presented in [7], [15], and [17]. Furthermore, the PMOS input is used because of the possibility of canceling the body effect in the PMOS devices.

C. Comparator

The design requirement of the comparator in the modulator is relaxed because the nonidealities of the comparator undergo noise shaping by the loop filter. Therefore, we employed a simple dynamic regenerative comparator. Fig. 11 shows a schematic of a regenerative comparator. This comparator consists of input transistors (M1 and M2), clock transistors (M5 and M6), precharge transistors (M9 and M10), and cross-coupled transistors (M3, M4, M7, and M8), which form a positive feedback loop. The operation of this comparator is

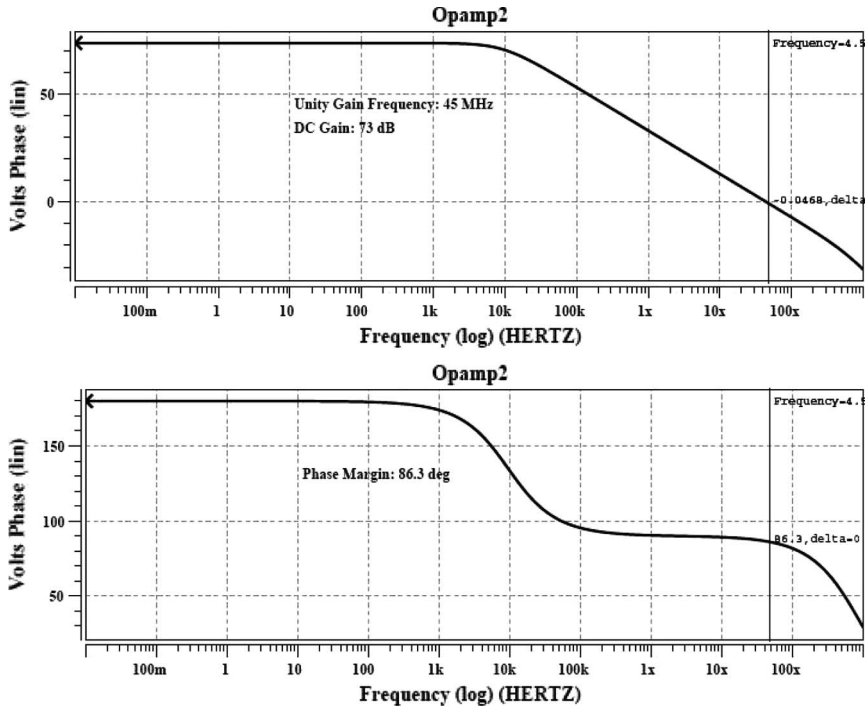

Fig. 10. AC simulation wave of Opamp2.

TABLE IV
SIMULATED RESULT OF OPAMPS

Parameter	Opamp1	Opamp2
Power supply voltage [V]	3	3
DC gain [dB]	73	73
Phase Margin [deg]	87.7	86.3
Slew Rate [V/μs]	86.7	63
Unity Gain Freq, F_u [MHz]	54	45
Effective load capacitance [pF]	6	2
Output Swing [Vpp]	± 2.2	± 2.2
Power Consumption [mW]	3.165	0.822

TABLE V
INPUT TRANSISTOR SIZES IN OPAMPS

Opamp version	Input transistors	Width/Length size [μm]
1	M1, M2	160/0.8
2	M1, M2	40/0.8

described as follows. When clock Φ1 is low, the cross-coupled transistors are reset, and the output nodes ($Vo+$ and $Vo-$) are both pulled to VDD by the precharge transistors. Then, when clock Φ1 is high, the latch enters the regeneration phase. During the regeneration phase, the small imbalance of the input signal is regenerated to a rail-to-rail value.

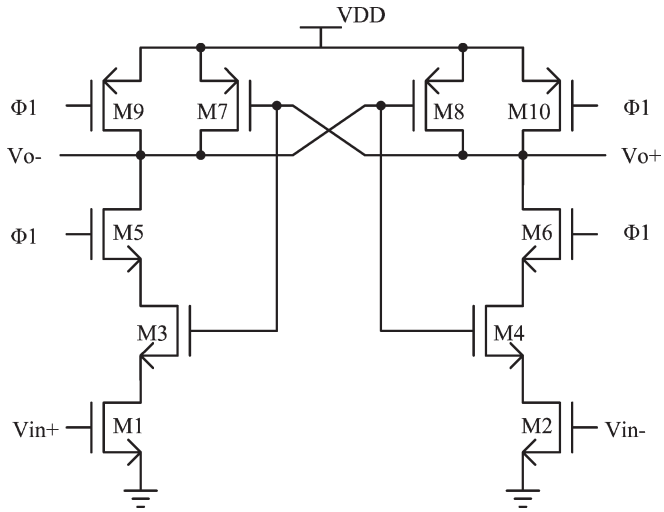

Fig. 11. Regenerative comparator circuit.

D. Clock Generator

At least one pair of nonoverlapping clocks is essential in switched-capacitor circuits. These clocks determine when charge transfers among capacitors occur, and they must be nonoverlapping to guarantee that the charge is not inadvertently lost. Fig. 12 shows the schematic of the clock generator generating clocks Φ1, Φ2, Φ1d, and Φ2d. The clock generator consists of two NOR gates and several inverters. Two NOR gates and inverter 0 (Inv0) generate a two-phase nonoverlapping clock. The inverter pairing with the outputs of each NOR gate is a common method for increasing the time when all four clock signals are low. As shown in Fig. 12, $C_{\rm d}$ is a 100-fF capacitor and controls the delay time between the two clock phases. $C_{\rm con}$, in parallel with $C_{\rm d}$, is controlled by the switch $S_{\rm test}$ and

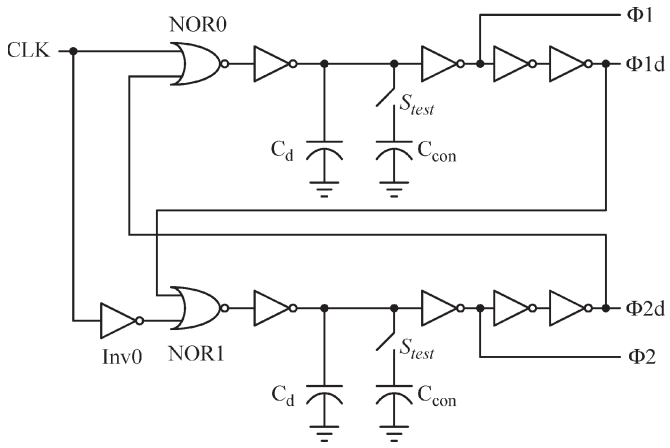

Fig. 12. Clock generator circuit.

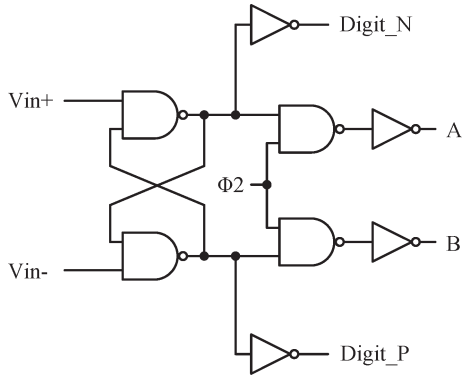

Fig. 13. SR latch.

provides additional flexibility in adjusting the nonoverlapping and delay times between the two clock phases.

E. SR Latch

The single-bit digital-to-analog-converter block in Fig. 2 is implemented with a switch network controlled by the comparator output value, as shown in Fig. 7. The set–reset (SR)-latch block in Fig. 7 has two functions. First, the SR latch holds the modulator output value. Second, it drives the feedback reference switches. Fig. 13 shows the schematic of the SR-latch block in accomplishing the two functions mentioned above. The SR-latch output values are synchronized with the Φ2 clock and change the signals (A and B) to drive the switches used in each feedback network. The Digit_P and Digit_N signals are connected to the digital output pad, and one of these signals is captured by the logic analyzer, as explained in Section IV.

F. Simulation Results

Fig. 14 shows the simulated output spectrum of the proposed modulator. The total number of points collected for spectrum analysis is 8192. In Fig. 14, the horizontal axis is the frequency, and the vertical axis is the power relative to a full-scale sine wave. The units on the vertical axis are in decibels. A solid line in Fig. 14 is a boundary line of the 20-kHz signal band. The spectrum shown in this figure corresponds to an input full-scale

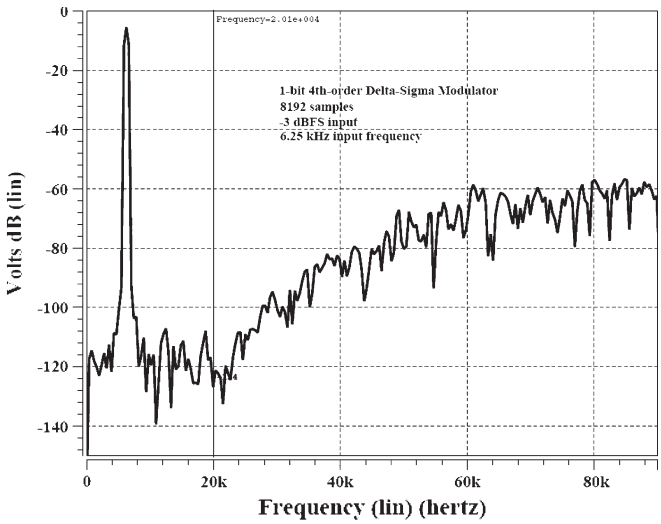

Fig. 14. Simulated output spectrum (8192 samples).

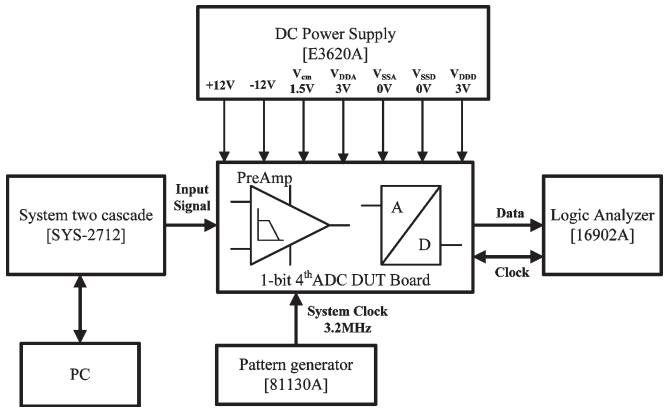

Fig. 15. Test setup.

sine wave of −3-dB, having a frequency of 6.25 kHz. We used an input frequency value of 6.25 kHz to analyze the effect of the third harmonic distortion in the signal band. The simulated peak SNDR obtained from HSPICE is 97.2 dB. Additionally, we obtained the various simulated SNDRs of 94.4, 88.5, and 81.9 dB with the input amplitudes of −6, −10, and −20 dB, respectively.

IV. Experimental Results

A. Measurement Setup

Fig. 15 shows the test setup used to measure the performance of the modulator described in this paper. The input to the device under test (DUT) is generated using an Audio Precision SYS-2712 signal generator. The supply voltages are directly provided by an Agilent E3620 with a low-noise property. Seven supply voltages are supplied to the DUT board. Among these supply voltages, the analog power (V_{DDA}), the analog ground (V_{SSA}), and the common-mode voltage (V_{cm}) are supplied to the designed modulator. The modulator output bitstream is acquired by the high-quality Agilent 16902A logic analyzer. A 3.2-MHz system clock is supported using the Agilent 81130A pulse generator. The test board is shown in

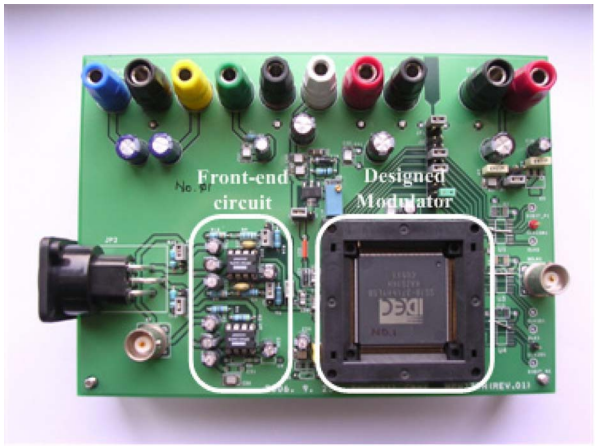

Fig. 16. Printed circuit board (PCB).

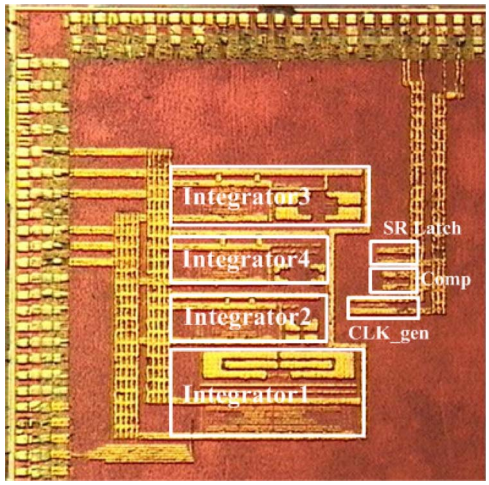

Fig. 17. Chip microphotograph.

Fig. 16 with the designed modulator in a socket. To reduce the possibility of digital noise interference, separate analog and digital planes, as well as decoupling capacitors, are used in the board [18].

B. Measurement Results

The proposed high-resolution delta–sigma modulator has been integrated using a one-poly four-metal (1P4M) 0.18-μm standard complementary metal–oxide semiconductor (CMOS) process. Fig. 17 shows a microphotograph of the chip. The guard ring between the analog and digital blocks in Fig. 17 separates them to avoid noise from the digital block. Absolute capacitor values are not critical in switched-capacitor designs. However, capacitor matching is of utmost importance since the capacitor's ratio is primarily responsible for the modulator's pole/zero locations [10]. Therefore, the common-centroid technique was used to give good component matching. The chip core size is 1.22 mm^2. The designed modulator operates at a single 3-V supply voltage, an F_s of 3.2 MHz, and an OSR of 80. Fig. 18 shows the measured SNR and SNDR versus the normalized input amplitude. The input frequency used to measure the modulator is 6.25 kHz. To effectively measure SNR and SNDR, we increased the amount of input

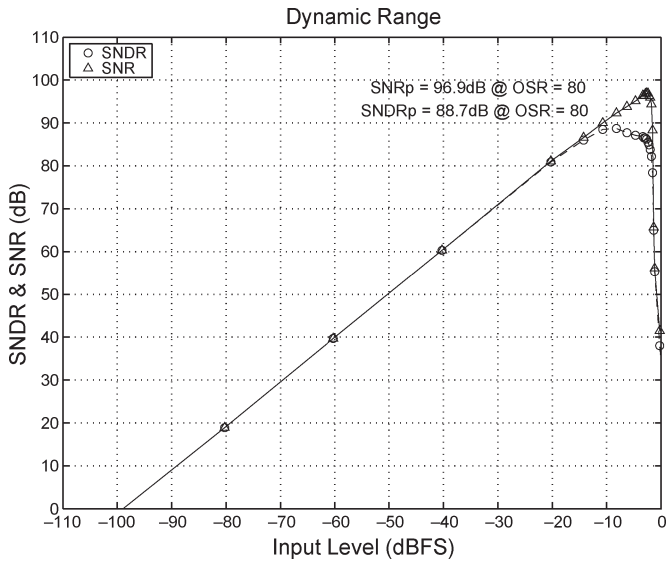

Fig. 18. Measured SNR and SNDR.

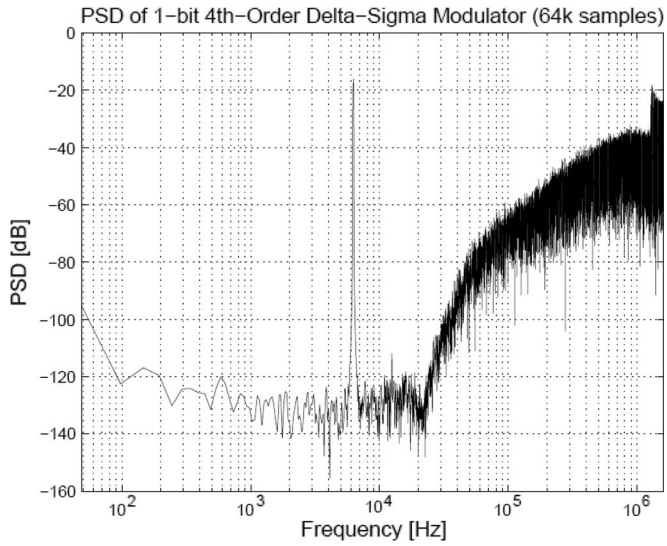

Fig. 19. Measured spectrum for a −14.2-dB input (65 536 samples).

amplitude by 20 dB from −100 to −10 dB. Next, we increased the amount of input amplitude by 1 dB from −10 to 0 dB to obtain more detailed data. The DR is 99 dB in the 20-kHz signal band. The peak SNR reaches 96.9 dB, while the peak SNDR reaches 88.7 dB. The measured peak SNDR dropped by about 10 dB lower than the result of HSPICE simulation. For the low input amplitudes, the measured SNDRs are about 2 or 3 dB lower than the results of HSPICE simulations. The total power consumption of the modulator is 5.6 mW.

Fig. 19 shows the measured output spectrum for a −14.2-dB sinusoid input signal. In this figure, we can observe that the noise is clearly attenuated by noise shaping inside the 20-kHz signal band. However, the SNDR is degraded due to the harmonic distortions caused by integrator saturations at large input signals. In addition, extra circuit nonidealities such as mismatches and the noise on the power supply rails are assumed to cause distortions. Table VI summarizes the measured performance of the chip.

TABLE VI
MEASUREMENT RESULT

Specification	Value
Number of orders	4
Oversampling ratio	80
Signal bandwidth	20 kHz
Sampling frequency	3.2 MHz
Peak SNDR	88.7 dB
Peak SNR	96.9 dB
ENOB	15.8 bits
Dynamic range	99 dB
Supply voltage	3 V
Core area	1.22 mm^2
Power consumption	5.6 mW
Technology	0.18 μm CMOS 1P4M

TABLE VII
COMPARISON OF FOM

Architecture	BW(kHz)	DR(dB)	$SNDR_P$(dB)	VDD(V)	P(mW)	FOM(dB)
ΔΣ: 2 (32-b) SC [19]	20	102	100	3.3	70.4	156.5
ΔΣ: 2 (4-b) Hybrid [20]	20	102	•	3.3	37.3	159.3
ΔΣ: 2 (4-b) Hybrid [21]	20	106	•	3.3	18	166.5
ΔΣ: 3 (1-b) SC [22]	25	88	85	1	0.95	162.0
ΔΣ: 2 (1-b) SC [23]	20	80	78	1	5.6	146.0
ΔΣ: 2 (1.5-b) - 2 (1-b) SC [24]	24	82	81	0.6	1	155.8
ΔΣ: 3 (1-b) SC [25]	16	77	62	0.9	0.04	163.0
ΔΣ: 2 (1-b) SC [26]	10	83	80	0.9	0.2	159.9
ΔΣ: 4 (1-b) SC [This work]	20	99	88.7	3	5.6	164.5

The FOM of a delta–sigma modulator is defined as [7]

$$\text{FOM} = \text{DR}_{\text{dB}} + 10\log\left(\frac{\text{signal bandwidth}}{\text{power}}\right). \qquad (9)$$

This FOM uses a decibel scale to facilitate calculations. Table VII shows the performance comparison of the state-of-the-art delta–sigma modulators with similar bandwidths. In Table VII, our proposed modulator has 164.5-dB FOM.

V. CONCLUSION

In this paper, we have presented an implementation of a delta–sigma modulator for high-performance sensor applications. We have obtained a 99-dB maximum DR from the proposed modulator with a loop filter composed of both feedback and feedforward paths. The modulator consumes 5.6 mW from a single 3-V power supply. The core area is 1.22 mm^2. The IC is fabricated in a 0.18-μm CMOS 1P4M process. Compared with the other delta–sigma modulators listed in Table VII, our modulator achieves a good FOM, which indicates that both power and performance are well optimized.

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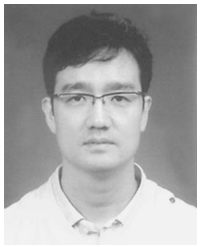
Youngkil Choi (S'06) received the B.S. and M.S. degrees in electrical engineering and computer science from Hanyang University, Ansan, Korea, in 2004 and 2006, respectively. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, Hanyang University.

His research interests include low-power high-performance sigma–delta modulators and mixed-signal integrated circuits.



Jeongjin Roh (M'01) received the B.S. degree in electrical engineering from Hanyang University, Ansan, Korea, in 1990, the M.S. degree in electrical engineering from Pennsylvania State University, University Park, in 1998, and the Ph.D. degree in computer engineering from the University of Texas at Austin in 2001.

From 1990 to 1996, he was with the Samsung Electronics, Kiheung, Korea, as a Senior Circuit Designer for several mixed-signal products. From 2000 to 2001, he was with Intel Corporation, Austin, as a Senior Analog Designer for delta–sigma data converters. Since 2001, he has been a member of the faculty of the Department of Electrical and Computer Engineering, Hanyang University. His research interests include oversampled delta–sigma converters and power-management circuits.

Hyungdong Roh (S'06) received the B.S. and M.S. degrees in electrical engineering and computer science from Hanyang University, Ansan, Korea, in 2005 and 2007, respectively. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, Hanyang University.

His current research interests include low-voltage low-power sigma–delta analog-to-digital converter.

Hyunseok Nam (S'06) was born in On-jeong, Korea, in 1980. He received the B.S. degree from Hallym University, Chuncheon, Korea, in 2005 and the M.S. degree in electrical engineering and computer science from Hanyang University, Ansan, Korea, in 2007. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, Hanyang University.

His research interests include the design of switch-mode power converters and mixed-signal integrated circuits.

Songjun Lee received the B.S. and M.S. degree in electronics engineering from the Hanyang University, Ansan, Korea, in 1994 and 1996, respectively, and Ph.D. degree in computer engineering from the University of Texas at Austin in 2002.

From 2003 to 2005, he was with the Telecommunication R&D Center, Samsung Electronics, Suwon, Korea, as a Senior Circuit Designer for mobile station modems. Since 2005, he has been a member of the faculty of the Department of Electrical and Computer Engineering, Hanyang University. His research interests include sensor fusion systems and sensor networks.