A 1.2-V 4.2-ppm/°C High-Order Curvature-Compensated CMOS Bandgap Reference

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***Abstract*—This study presents a high-precision CMOS bandgap reference (BGR) circuit with low supply voltage. The proposed BGR circuit consists of two BGR cores and a curvature correction circuit, which includes a current mirror and a summing circuit. Two BGR cores adopt conventional structures with the curvature-down characteristics. A current-mirror circuit is proposed to implement one of the BGR cores to have the curvature-up characteristic. Selection of the appropriate resistances in the BGR cores results in one reference voltage with a well balanced curvature-down characteristic and another reference voltage with an evenly balanced curvature-up characteristic. The summation of these reference voltages is proposed to achieve a high-order curvature compensation. This curvature correction circuit causes the proposed BGR circuit without any trimming to show a measured temperature coefficient (TC) as low as 4.2 ppm/°C over a wide temperature range of 160 °C (−40 ∼ 120 °C) at a power supply voltage of 1.2 V. The average TC for 8 random samples is approximately 9.3 ppm/°C. The measured power-supply rejection ratio (PSRR) of −30 dB is achieved at the frequency of 100 kHz. The total chip size is 0.063 mm^2 with a standard 0.13-μm CMOS process.**

***Index Terms*—Bandgap reference, high-order curvature compensation, high-precision, low voltage, temperature coefficient.**

I. Introduction

BANDGAP reference circuits have broad applications in purely analog and mixed-mode circuits. As reference voltages, their accuracy plays a vitally important role in determining the performance of subsequent circuits. For example, BGR circuits are utilized in analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), which require high-accuracy reference voltages to provide high-resolution and high-speed data conversion. Therefore, the fabrication of high-precision BGR circuits has become a great concern, and several high-order curvature-compensation techniques have been developed to improve the accuracy [1]–[7].

The increasing demand for portable equipment has led to scaling down of supply voltage due to the reduction in size of the CMOS transistors. However, the threshold voltages are not scaled down to the same extent as the supply voltage. The conventional BGR circuits have an approximate reference voltage of 1.25 V [8]–[10], so that use of the conventional structures with a power supply voltage lower than 1.2 V is not possible. This significantly increases the difficulty of designing a high-accuracy BGR circuit with a low supply voltage.

This study presents a new high-order curvature-compensated BGR circuit with low supply voltage. The proposed BGR circuit has stable output reference voltages approximately 0.73 V and a TC as low as 4.2 ppm/°C at a 1.2-V supply voltage.

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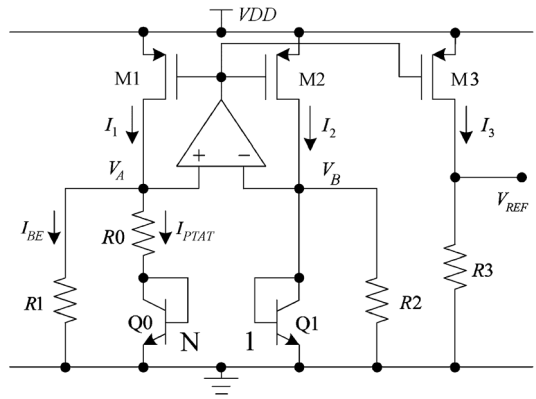

Fig. 1. Bandgap reference circuit with low power supply voltage [13].

II. Conventional Bandgap Reference

In general bandgap topologies, a diode-connected bipolar transistor (BJT) is chosen as the main element due to its good temperature-dependent characteristics, as presented in Fig. 1. When BJTs are biased in the forward active region, the base-emitter voltage V_{BE} can be expressed as [10]–[12]

$$V_{BE}(T) = V_{G0}(T_r) - [V_{G0}(T_r) - V_{BE}(T_r)]\,T/T_r - (\eta - \xi)V_T ln\left(\frac{T}{T_r}\right), \quad (1)$$

where $V_{G0}(T_r)$ is the bandgap voltage at reference temperature T_r, ξ is the order of temperature dependence of collector current, and η is a temperature-independent and process-dependent constant. $V_T = kT/q$ is the thermal voltage, k is Boltzmann's constant, and q is the charge of an electron. In (1), $V_{G0}(T_r)$ is constant at the temperature of T_r, $[V_{G0}(T_r) - V_{BE}(T_r)]T/T_r$ is the first-order temperature-dependent part, and $(\eta - \xi)V_T ln(T/T_r)$ is the high-order nonlinearity. Thus, a correction voltage is required to cancel, or at least reduce, the temperature dependence. V_T with a proper coefficient M is generally used as the correction voltage and $V_{REF} = V_{BE} + MV_T$. V_{BE} can be expanded by the Taylor series as

$$V_{BE} = a_0 + a_1 T + (a_2 T^2 + \cdots + a_n T^n), \quad (2)$$

where a_2 is -3.05×10^{-7} V/K^2 to 0 in the range of 150 K (−123 °C) to 400 K (127 °C) [10]. Therefore, the conventional structure has a curvature-down characteristic.

As mentioned in the introduction, the conventional structure cannot work with a supply voltage lower than 1.2 V, so the topology shown in Fig. 1 is developed [13], and $V_{REF} = R3/R1 \cdot [R1ln(N)V_T/R0 + V_{BE}]$, where $R1/R0 \cdot ln(N)$ is the temperature-independent factor of M mentioned above. In order to obtain high accuracy, the high-order compensation is expected. Fig. 2(a) shows an efficient high-order compensation technique that has two reference currents, I_{REF1} and I_{REF2} [5]. They are realized by NPN BJTs and PNP BJTs, respectively. $I_{REF2} - I_{REF1}$ is used to obtain the high-order compensation, and the reference voltage is expressed as

$$V_{REF} = R_{REF}\left[\left(K_2\frac{V_{BE\_npn}}{R_{1\_npn}} - K_1\frac{|V_{BE\_pnp}|}{R_{1\_pnp}}\right) + \frac{kT}{q}\left(K_2\frac{ln(N\_npn)}{R_{3\_npn}} - K_1\frac{ln(N\_pnp)}{R_{3\_pnp}}\right)\right], \quad (3)$$

where R_{REF} is the output reference resistor, and V_{BE_npn} and V_{BE_pnp} are the base-emitter voltages of the NPN BJT and PNP BJT, respectively. N_npn and N_pnp are the ratios of the NPN BJTs and PNP BJTs. R_{3_npn} and R_{3_pnp} are resistors flowing the proportional-to-absolute-temperature (PTAT) currents. R_{1_npn} and R_{1_pnp} are resistors flowing the currents of I_{BE} for the NPN and PNP BJT, respectively. K_1 and K_2 are temperature-independent coefficients. By using (2), the first term in (3) can be expressed as

$$\begin{aligned} &K_2'V_{BE\_npn} - K_1'|V_{BE\_pnp}| \\ &\quad = (K_2'a_{0\_npn} - K_1'|a_{0\_pnp}|) + (K_2'a_{1\_npn} - K_1'|a_{1\_pnp}|)\,T \\ &\qquad + \left[(K_2'a_{2\_npn} - K_1'|a_{2\_pnp}|)\,T^2 + \cdots \right. \\ &\qquad \left. + (K_2'a_{n\_npn} - K_1'|a_{n\_pnp}|)\,T^n\right], \end{aligned} \quad (4)$$

where $K_2' = K_2R_{REF}/R_{1\_npn}$, and $K_1' = K_1R_{REF}/R_{1\_pnp}$. In order to obtain a reference voltage, K_2' should be greater than K_1', otherwise V_{REF} is close to zero. Thus, a constant voltage $K_2'a_{0\_npn} - K_1'|a_{0\_pnp}|$ is obtained by selecting proper K_2' and K_1'. The first-order term $(K_2'a_{1\_npn} - K_1'|a_{1\_pnp}|)T$ is compensated by the term of $R_{REF}(kT/q)[K_2ln(N\_npn)/R_{3\_npn} - K_1ln(N\_pnp)/R_{3\_pnp}]$ in (3). However, the compensation of the high-order part is not as sufficient as that of the first-order part due to the nonzero coefficient of $K_2' - K_1'$.

The second-order term is discussed in detail here, since it is the most significant term compared with other higher-order terms. From (4), the second-order term $(K_2'a_{2\_npn} - K_1'|a_{2\_pnp}|)T^2$ is obtained. Fig. 2(b) shows the relationship between the output reference current I_{REF} and K_1'/K_2', where the same absolute coefficients for NPN and PNP BJTs are assumed. For the relationship of $y1$, when $K_1'/K_2' = 30\%$ (which implies that only 30% of second-order term is compensated), the reference current is approximately 14 μA. If 0.7 V is the goal of the reference voltage, then reference resistances of 50 kΩ are required. When K_1'/K_2' becomes 99% (which means that 99% of second-order term is compensated), the reference current is only 0.2 μA. For the 0.7-V reference voltage, reference resistances of 3.5 MΩ are required. In this condition, the currents in transistors M2 and M3 are around 20 μA $[0.2/(1-99\%) = 20\ \mu\text{A}]$. Therefore, we say that the more sufficient compensation requires significantly large reference resistances; however, this greatly increases the chip area and noise. High-accuracy compensation with a reasonable output reference current and resistance is achieved using the relationship of $y2$ shown in Fig. 2(b). For 99% compensation, the output reference current is 8.2 μA. Nevertheless, huge currents are necessary in transistors M2 $[8.2/(1-99\%) = 820\ \mu\text{A}]$ and M3 $[99\% \times 8.2/(1-99\%) = 811.8\ \mu\text{A}]$. Consequently, we propose a more efficient compensation technique in this study in order to improve the accuracy and achieve more complete compensation with generic resistance and currents.

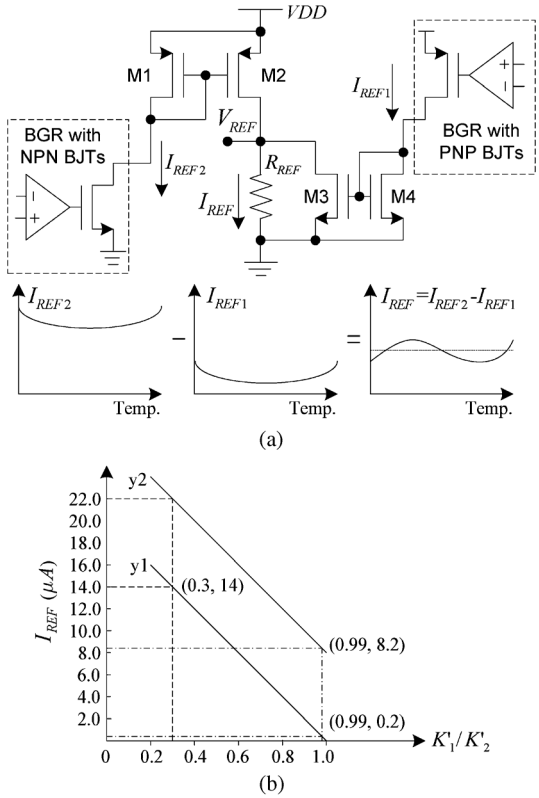

Fig. 2. (a). Curvature-compensation technique [5]. (b). Output reference current versus K_1'/K_2'.

III. Proposed Bandgap Reference Circuit

A. Design Consideration of BGR

The BJTs occupy the main area in the BGR circuits, while the smaller "N" of BJTs means that large resistances are necessary to obtain the factor of M mentioned above. The resistor is another main element that consumes chip area. Since the BGR circuit is a sensitive block, a slight mismatch may significantly affect the accuracy of the output reference voltage. Trading off the area and the matching, N of 8 is chosen in this study. In addition, components with a deep n-well layer are chosen, since this can efficiently separate the p-substrate for different circuits and then block the noise from other subsequent circuits. Since the supply voltage is low, two-stage operational amplifiers (opamp) are selected in this BGR circuit. The advantage of high-DC gain for the two-stage opamp at a low supply voltage gives BGR circuit a high loop gain, which makes the nodes V_A and V_B a good virtual ground in Fig. 1.

B. Principle of the Proposed Compensation Technique

Fig. 3 shows the new high-order curvature-compensation technique of the proposed BGR circuit. It contains two conventional low-supply-voltage BGR cores (A and B) and a

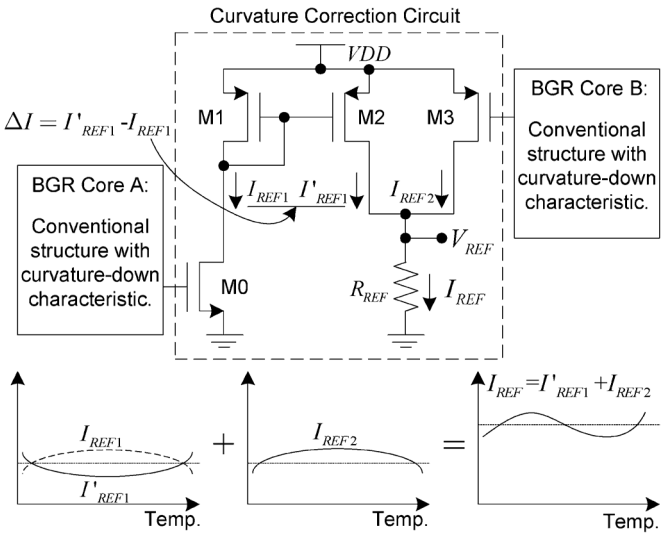

Fig. 3. New curvature-compensation technique of the proposed BGR circuit.

curvature correction circuit, which includes a current-mirror block and a summing circuit. BGR core A has a reference current of I_{REF1} and BGR core B has a reference current of I_{REF2}. Both I_{REF1} and I_{REF2} only cancel out the first-order temperature-dependent terms and have curvature-down characteristics. Their accuracy is not high due to the high-order nonlinearity errors. However, when I_{REF1} passes through a current-mirror circuit (M1 and M2), then a new reference current I'_{REF1}, with a curvature-up characteristic, is generated. I'_{REF1} with a curvature-up characteristic and I_{REF2} with a curvature-down characteristic are summed together and their high-order nonlinearity terms are well compensated for each other. Therefore, the proposed technique achieves high-order curvature compensation.

As shown in Fig. 3, the difference in the drain and source voltage for transistors M1 and M2 causes a difference in the current $\Delta I = I'_{REF1} - I_{REF1}$. The ΔI is a function of the temperature-dependent parameters, the carrier mobility μ, and the threshold voltage V_{TH}. Their temperature-dependent features and the square law characteristic of transistors result in the generation of a reference current with a curvature-up characteristic. In following part, the curvature-up technique will be analyzed in detail. The drain current of transistors working in saturation region can be expressed by [14]

$$I_D \approx \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(|V_{GS}| - |V_{TH}|\right)^2\left(1+\lambda|V_{DS}|\right), \quad (5)$$

where C_{ox} is the gate oxide capacitance per unit area, and W and L are the width and length of transistors, respectively. λ is the channel-length modulation coefficient, and it is smaller for longer channels. μ is the temperature function of carrier mobility, and it is given by [15].

$$\mu = \mu(T_0)\left(\frac{T}{T_0}\right)^{\beta_\mu}, \quad (6)$$

where β_μ is the temperature coefficient. $\beta_\mu = -1.2$ for PMOS transistor and $\beta_\mu = -1.9$ for NMOS transistor, when the concentrations increase above 10^{17} cm^{-3}. $\beta_\mu \approx -2$ for NMOS devices, when the concentrations are about $10^{15} - 10^{16}$ cm^{-3} [16]. Therefore, for the concentrations of about $10^{15} - 10^{16}$ cm^{-3}, assuming β_μ of -1.3 is reasonable for PMOS devices. Overall, recent techniques have used the concentrations of $10^{15} - 10^{18}$ cm^{-3}, so we can consider β_μ for PMOS devices is approximately -1.3 and β_μ for NMOS devices is approximately -2. T_0 is the reference temperature. The magnitude of transistors threshold voltage is approximated as a linear function of temperature, and can be modeled as [15]–[17]

$$|V_{TH}| = |V_{TH}(T_0)| + \beta_{TH}(T - T_0), \quad (7)$$

where β_{TH} is the temperature coefficient, its value is technology dependent, and the most frequently used figure is -2 mV/°C [16]. As presented in Fig. 4, according to (5) an ideal current I flowing transistor M1 is expressed as

$$I \approx \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(|V_{GS}| - |V_{TH}|\right)^2\left(1+\lambda|V_{GS}|\right), \quad (8)$$

where $V_{DS} = V_{GS}$, due to the diode-connection of M1. For simplicity of analysis, we assume an ideal current, which does not vary with temperature, as has been done in [16]. Therefore, for the given ideal current I, $\partial I/\partial T = 0$. The function of $|V_{GS}|$ with (6) and (7) can be expressed as follows:

$$\begin{aligned}|V_{GS}| &\approx |V_{TH}| + \frac{2\mu\left(\partial|V_{TH}|/\partial T - \partial|V_{GS}|/\partial T\right)}{\partial\mu/\partial T} \\ &\approx |V_{TH}(T_0)| + \beta_{TH}(T - T_0) + \frac{2b\beta_{TH}T}{\beta_\mu}, \quad (9)\end{aligned}$$

where $\partial|V_{GS}|/\partial T \approx (1-b)\partial|V_{TH}|/\partial T$, and b is close to 0. The output reference current I' in Fig. 4 is given by

$$I' \approx \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(|V_{GS}| - |V_{TH}|\right)^2\left[1+\lambda(V_{DD} - V_{REF})\right], \quad (10)$$

Thus, with (6)–(10), the difference between the output current and reference current ΔI can be presented as

$$\begin{aligned}\Delta I = I' - I \approx \frac{\lambda}{2}C_{ox}\mu(T_0)\left(\frac{T}{T_0}\right)^{\beta_\mu}\frac{W}{L}\frac{4b^2\beta_{TH}^2T^2}{\beta_\mu^2}\Big[(V_{DD} - \\ V_{REF} - |V_{TH}(T_0)|) - \beta_{TH}(T - T_0) - \frac{2b\beta_{TH}T}{\beta_\mu}\Big], \quad (11)\end{aligned}$$

As mentioned above, $\beta_{TH} = -2$ mV/°C and $\beta_\mu = -1.3$ for PMOS devices. For simplicity, assuming $\beta_\mu = -1.0$, so $\partial^2(\Delta I)/\partial T^2$ can be presented as

$$\frac{\partial^2(\Delta I)}{\partial T^2} \approx \frac{4\lambda C_{ox}\mu(T_0)T_0b^2\beta_{TH}^2}{\beta_\mu^2}\frac{W}{L}\left[-\beta_{TH}\left(1+\frac{2b}{\beta_\mu}\right)\right] > 0, \quad (12)$$

since $\beta_{TH} < 0$, and $1 + 2b/\beta_\mu > 0$. So we can obtain

$$\frac{\partial^2 V'_{REF}}{\partial T^2}(>0) \propto \frac{\partial^2 I'}{\partial T^2} \propto \frac{\partial^2(\Delta I)}{\partial T^2}, \quad (13)$$

where $V_{REF} = I'R_{REF}$ as presented in Fig. 4. With the ideal input reference current I and the ideal reference resistor R_{REF}, the output reference voltage V_{REF} shows curvature-up characteristic and its second derivative, $\partial^2 V_{REF}/\partial T^2$, is positive versus temperature. Therefore, the current-mirror circuit with PMOS transistors obtains a curvature-up characteristic.

In (7), the threshold voltage is approximately modeled as a linear function of temperature, and the temperature coefficient β_{TH} is constant. However, β_{TH} is actually a function of temperature, and its more accurate model and first derivative are

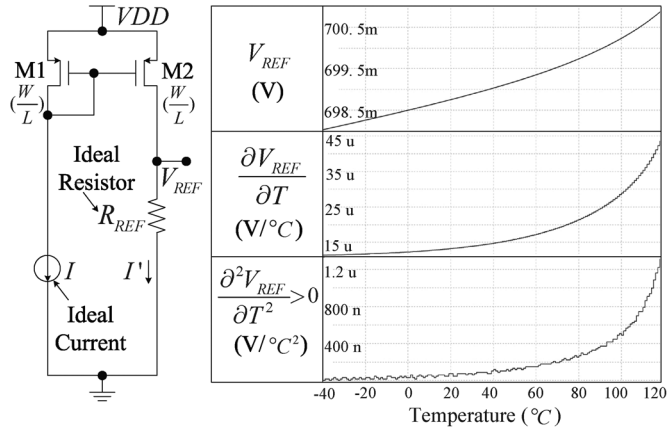

Fig. 4. The curvature-up characteristic due to the temperature dependence of transistors and the simulation results.

given by [17]

$$V_{TH} = \phi_{ms} \pm \phi + \Delta V_T(N_i) \pm \gamma(N_S, t_{ox}, L, W)\left(|V_{SB}| + \phi + V_o\right)^{\frac{1}{2}}, \quad (14)$$

$$\frac{\partial V_{TH}}{\partial T} = \frac{\partial}{\partial T}(\phi_{ms} \pm \phi) \pm \frac{\gamma}{2\left(|V_{SB}| + \phi + V_o\right)^{\frac{1}{2}}}\frac{\partial \phi}{\partial T}, \quad (15)$$

where the $+$ or $-$ sign refers to n-channel or p-channel devices, respectively. ϕ_{ms} is the contact potential difference between gate and substrate, ϕ is the associated band bending, V_o is a correction term for the threshold shift implant, γ is the substrate backbias factor, which depends on the substrate doping N_S, the gate insulator thickness t_{ox} and the channel length L and width W. V_{SB} is the source-substrate bias. Therefore, we can assume that

$$|V_{TH}| \approx |V_{TH}(T_0)| + \beta_{TH1}(T - T_0) + \beta_{TH2}(T - T_0)^2, \quad (16)$$

where β_{TH1} and β_{TH2} are the first- and second-order temperature coefficients, respectively. Therefore, (9) becomes

$$|V_{GS}| \approx |V_{TH}(T_0)| + \beta_{TH1}(T - T_0) + \beta_{TH2}(T - T_0)^2 + \frac{2b\left[\beta_{TH1} + 2\beta_{TH2}(T - T_0)\right]T}{\beta_\mu}. \quad (17)$$

By using (17), ΔI in (11) can be expressed as

$$\Delta I \approx \frac{\lambda}{2} C_{ox}\mu(T_0)\left(\frac{T}{T_0}\right)^{\beta_\mu}\frac{W}{L}\frac{4T^2b^2[\beta_{TH1} + 2\beta_{TH2}(T - T_0)]^2}{\beta_\mu^2} \left\{(V_{DD} - V_{REF} - |V_{TH}(T_0)|) - \beta_{TH1}(T - T_0) - \beta_{TH2}(T - T_0)^2 - \frac{2b\left[\beta_{TH1} + 2\beta_{TH2}(T - T_0)\right]T}{\beta_\mu}\right\}, \quad (18)$$

When $\beta_\mu = -2$, ΔI can be presented as

$$\Delta I \approx \frac{2\lambda C_{ox}\mu(T_0)T_0^2Wb^2}{\beta_\mu^2 L}\left[\beta_{TH1}^2 + 4\beta_{TH1}\beta_{TH2}(T - T_0) + 4\beta_{TH2}^2(T - T_0)^2\right]\left[(V_{DD} - V_{REF} - |V_{TH}(T_0)|) - \beta_{TH1}(T - T_0) - \frac{2b\beta_{TH1}}{\beta_\mu}T - \beta_{TH2}(T - T_0)^2 - \frac{4b\beta_{TH2}}{\beta_\mu}(T - T_0)T\right]. \quad (19)$$

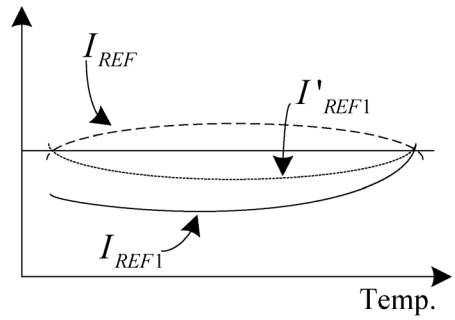

Fig. 5. Reference current varying with the temperature at different conditions.

The second derivative $\partial^2(\Delta I)/\partial T^2$ can be obtained as

$$\frac{\partial^2(\Delta I)}{\partial T^2} \approx \alpha\beta_{TH2}^2\left[4A - \frac{\beta_{TH1}^2}{\beta_{TH2}}\left(5 + \frac{12b}{\beta_\mu}\right) + 24\beta_{TH1}T_0\left(1 + \frac{2b}{\beta_\mu}\right) - 24\beta_{TH2}T_0^2\left(1 + \frac{2b}{\beta_\mu}\right)\right], \quad (20)$$

where

$$\alpha = \frac{4\lambda C_{ox}\mu(T_0)T_0^2Wb^2}{\beta_\mu^2 L} > 0, \quad (21)$$

$$A = V_{DD} - V_{REF} - |V_{TH}(T_0)|, \quad (22)$$

where the higher-order terms are ignored for simplicity. Therefore, the proper choice of the reference voltage V_{REF} ensures that $\partial^2(\Delta I)/\partial T^2 > 0$, even when $\beta_{TH2} > 0$. Thus, for PMOS transistor, the third-order term is generated, which can be used to compensate the high-order part in BGR circuit. On the other hand, even when this β_μ is equal to -2, ΔI can have a positive second-order term and achieve a curvature-up characteristic. For NMOS transistors, $\beta_\mu \approx -2$, and we can achieve that $\partial^2(\Delta I)/\partial T^2 > 0$. In other words, the current-mirror circuit with NMOS transistors also can have a curvature-up characteristic. Consequently, the current-mirror circuits are proposed to realize curvature-up characteristic in this study.

As demonstrated in Fig. 3, the given current I_{REF1} passes through the current-mirror circuit consisting of the PMOS transistors M1 and M2, so that I'_{REF1} in M2 achieves a positive second-order temperature-dependent term. The balanced current I'_{REF1} with a curvature-up characteristic is obtained through selection of appropriate resistances in BGR core A. At the same time, by selecting an appropriate length for the transistors, different levels of ΔI can be obtained. The summing circuit is shown in Fig. 3, where the summed current of I_{REF} and the reference resistor of R_{REF} produce the output reference voltage of V_{REF}. Thus, summing the curvature-up current of I'_{REF1} and the curvature-down current of I_{REF2} generates a high-precision reference voltage, as shown in Fig. 3.

C. Two BGR Cores

The proposed technique requires two BGR cores, since the curvature with a well balanced curvature-up characteristic is obtained through selection of appropriate resistor values. From (11), we can obtain the first derivative $\partial\Delta I/\partial T \neq 0$, so the first-order term error is generated in the current-mirror circuit. Consequently, new resistances are required to compensate for this error. As presented in Fig. 5, I_{REF} is the reference current of conventional BGR circuit and it has a well balanced curvature-down characteristic. I_{REF} then passes through the mirror-

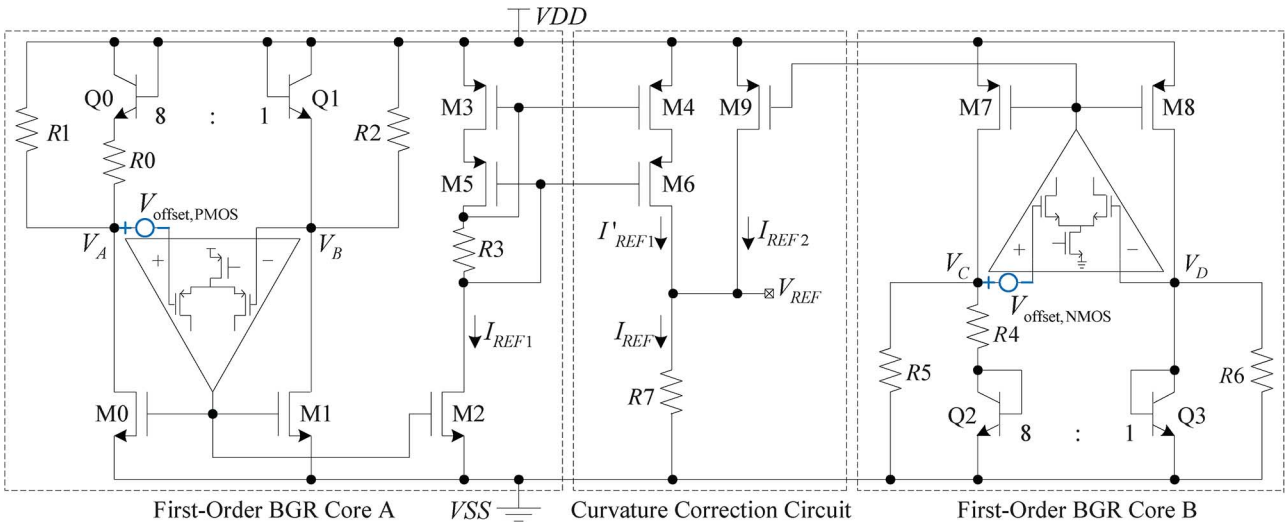

Fig. 6. Implementation of proposed bandgap reference circuit.

current circuit, as mentioned above, and I_{REF1} is obtained. However, it has a first-order error from the current-mirror circuit, and this error makes the peak-to-peak current of I_{REF1} obviously larger than the peak-to-peak current of I_{REF}. Selection of appropriate new resistances achieves a new reference current I'_{REF1} with an evenly balanced curvature-up characteristic and smaller peak-to-peak current. Therefore, we can see the difficulty in achieving one balanced curvature with a curvature-up characteristic and another balanced curvature with a curvature-down characteristic when using the same BGR core with the same resistances.

D. Implementation of the Proposed BGR Circuit

Fig. 6 presents the implementation of the proposed BGR circuit including two BGR cores and a curvature correction circuit. BGR core A uses a self-biased, two-stage opamp with PMOS-input transistors. BGR core B uses a self-biased, two-stage opamp with NMOS-input transistors. In BGR core A, $R1$ and $R2$ have the same resistances, and M0, M1, and M2 have the same size for the same current flow. The opamp forces the voltages of V_A and V_B to be equal and the reference current of I_{REF1} can be expressed as

$$I_{REF1} = \frac{V_T ln(N)}{R0} + \frac{V_{BE1}}{R1} = \frac{1}{R1}\left[\frac{R1 ln(N)}{R0} V_T + V_{BE1}\right], \tag{23}$$

where I_{REF1} with first-order compensation has the curvature-down characteristic. With the cascode current-mirror circuit (M3, M5, M4, and M6), a well balanced curvature-up reference current of I'_{REF1} is obtained by selecting appropriate resistor values. I'_{REF1} can be expressed as

$$I'_{REF1} = \frac{1}{R1}\left\{\frac{R1 ln(N)}{R0} V_T + V_{BE1} + [V(T) + V_h]\right\}, \tag{24}$$

where $V(T)$ is the first-order term and V_h is the high-order compensation term from the current-mirror curvature-up technique. $V(T)$ is canceled out by selecting the appropriate resistances for $R0$ and $R1$. The cascode current-mirror structure is used as one factor to decide the level of channel-length modulation, so a more appropriate V_h can be achieved. For BGR core B, $R5$ and $R6$ have the same resistances and transistors M7, M8, and M9 have the same size. In addition, we choose the same resistances of $R0$ and $R4$ to obtain the similar PTAT currents for BGR cores A and B. The opamp forces the voltages of V_C and V_D to be equal and the reference current I_{REF2} can be given by

$$I_{REF2} = \frac{V_T ln(N)}{R4} + \frac{V_{BE2}}{R5} = \frac{1}{R5}\left[\frac{R5 ln(N)}{R4} V_T + V_{BE2}\right]. \tag{25}$$

TABLE I
COMPONENTS SIZES OF THE PROPOSED BGR CIRCUIT

Component	Parameter
M0, M1, M2	W=4 μm, L=2 μm
M3, M4, M5, M6, M18, M19	W=20 μm, L=2 μm
M7, M8, M9, M20	W=10 μm, L=2 μm
Q1, Q3 (NPN BJT, Base Area)	1 $\times$(2 μm $\times$ 2 μm)
Q0, Q2 (NPN BJT, Base Area)	8 $\times$ (2 μm $\times$ 2 μm)
Unit resistor R_u	9.67 kΩ
$R0$, $R4$	14.51 kΩ (R_u + $R_u \| R_u$)
$R1$, $R2$	127.36 kΩ ($13R_u$+ $R_u \| R_u \| R_u \|$ $R_u \| R_u \| R_u$)
$R5$, $R6$	132.52 kΩ ($13R_u$+ $R_u \|$ R_u+ $R_u \| R_u \| R_u \| R_u \| R_u$)
$R7$	38.69 kΩ ($4R_u$)

Due to the negative coefficient of high-order nonlinearity term, I_{REF2} has the curvature-down characteristic. Then, through the summing circuit in Fig. 6, the proposed reference voltage V_{REF} can be presented as follows:

$$\begin{aligned} V_{REF} &= \frac{R7}{R1}\left\{\frac{R1 ln(N)}{R0} V_T + V_{BE1} + [V(T) + V_h]\right\} \\ &\quad + \frac{R7}{R5}\left[\frac{R5 ln(N)}{R4} V_T + V_{BE2}\right] \\ &= \left(\frac{R7}{R1} V_{C1} + \frac{R7}{R5} V_{C2}\right) + \left(\frac{R7}{R1} V_{h1} + \frac{R7}{R5} V_{h2}\right) \\ &= (M_1 V_{C1} + M_2 V_{C2}) + (M_1 V_{h1} + M_2 V_{h2}), \end{aligned} \tag{26}$$

where M_1 $(R7/R1)$ and M_2 $(R7/R5)$ are the temperature-independent factors due to the same type resistors. V_{C1} and V_{C2} are the temperature-independent reference voltages after

the first-order compensation. Therefore, the first term $M_1V_{C1}+M_2V_{C2}$ is a temperature-independent voltage. V_{h1} and V_{h2} are the high-order nonlinearity terms of BGR cores A and B, respectively. V_{h1} contains the high-order term of V_{BE} and the term V_h in (24). V_{h2} is the high-order term of V_{BE} in (25). As mentioned above, an appropriate V_{h1} ($V_{h1} \approx -V_{h2}$) can be obtained by selecting a suitable current-mirror structure and the proper transistor sizes in the current-mirror circuit. These two high-order nonlinearity terms with similar amplitudes and different signs are then summed and compensated for each other. Therefore, the precision of the output reference voltage is significantly improved by this efficient method.

Table I presents the sizes of components in the proposed BGR circuit. R_0 and R_4 have the same resistances, while $R1$ ($R2$) and $R5$ ($R6$) have slightly different values due to the first-order error generated in curvature-up technique. The unit resistor R_u (9.67 kΩ) is utilized to reduce the effect from the variation of resistances, and all resistors are generated by series connection and parallel connection of unit resistors, as shown in Table I.

As shown in Fig. 6, two cores are present in the proposed BGR circuit. According to the input range of the opamps in the two cores, PMOS-input and NMOS-input opamps are adopted for BGR cores A and B, respectively. Fig. 7 shows the implementation of the PMOS-input opamp, which includes a self-biased current with a start-up circuit. In Fig. 7, $K = 4$ is chosen in the self-biased current circuit, and a constant-g_m bias circuit is achieved to ensure a stable operation [19]. The transistor M0's body and source are connected together to eliminate the impact of the channel-length modulation [14]. The self-biased current is still a function of process and temperature, so different process corners are considered over a temperature range from −40 °C to 120 °C to ensure that all transistors operate at the correct region in a stable condition. To prevent the self-biased current circuit from working in the zero current dead-zone, a start-up circuit is utilized [19]. In this study, a two-stage amplifier is adopted to achieve a high DC gain. With a similar consideration, the same self-biased current circuit with a start-up circuit is applied for the NMOS-input opamp, as shown in Fig. 8.

As discussed earlier, $\Delta V_{BE} = V_T ln(N)$ is controlled by the opamp, which suffers from the unexpected error from the offsets of the opamp. Two kinds of offsets are possible: systematic offset and random offset. The systematic offset is mainly generated due to the limited gain of the opamp, and the higher DC-gain opamp can obtain a lower systematic offset [10]. Therefore, in the present study, two-stage amplifiers with Miller-compensation are used to reduce the error effects from the systematic offset, as shown in Figs. 7 and 8. In this design, at different process corners over the temperature range from −40 °C to 120 °C, the simulated DC gains of PMOS-input opamp and NMOS-input opamp are higher than 76 dB and 78 dB, respectively.

The random offset is mainly caused by the mismatch of components. An effective approach is doing careful layout to obtain a better matching. The common-centroid layout [14], [20] technique is adopted for the input transistors of opamps, and these input transistors are placed in a deep n-well, which ensures a similar environment as much as possible. The mismatch of the BJTs, mirror transistor, and resistors also generates an error for the reference voltage. Therefore, dummy transistors and BJTs are utilized at the sensitive places [14],

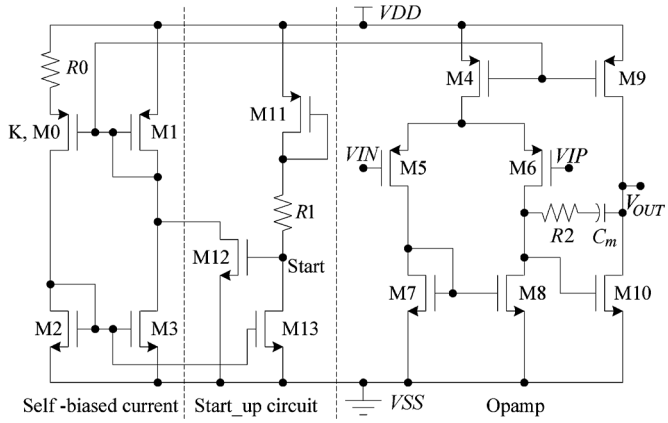

Fig. 7. Implementation of the PMOS-input operational amplifier.

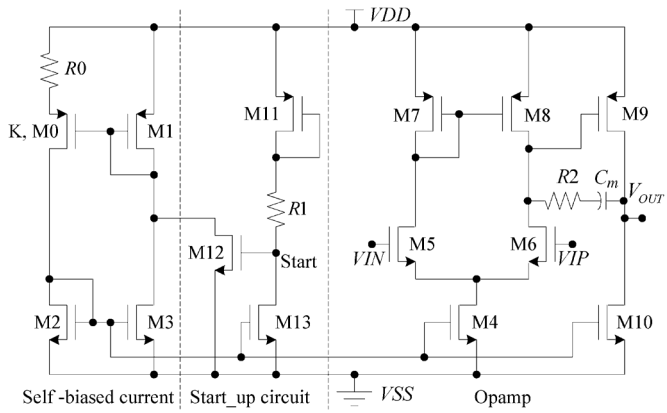

Fig. 8. Implementation of the NMOS-input operational amplifier.

TABLE II
THE SIMULATED RANDOM OFFSET EFFECT ON REFERENCE VOLTAGE

$V_{offset,PMOS}$/ $V_{offset,NMOS}$ (mV)	Ref. voltage (mV)	Peak-to-peak voltage (μV)
0 / 0	734.1	118 (Best)
0 / 2.5	742.2	248
0 / −2.5	725.9	381
2.5 / 0	726	287
−2.5 / 0	742.1	194
2.5 / −2.5	717.8	570 (Worst)
2.5 / 2.5	734.1	139
−2.5 / 2.5	750.3	379
−2.5 / −2.5	734.0	221

and the common-centroid layout technique is again widely used for the critical transistors and BJTs. Unit resistors are used to ensure an accurate ratio of the resistors, even though the resistor may have a maximum ±20–30% variation, as listed in Table I. Table II presents the simulated offset effects on the reference voltage, where Fig. 6 shows two offset voltages for the simulation. The worst case shows the peak-to-peak voltage of 570 μV (4.96 ppm/°C), which is still a good result. We can see that the offset also causes a shift in the reference voltages from 717.8 mV to 750.3 mV (32.5 mV). This shift of 32.5 mV may explain the voltage shifts in the measurement results (shown later in Fig. 13). The offset can be further reduced by using large size transistors at the cost of large silicon area. Since the matching property depends on the inverse of the square root of the area [14], the tradeoff between the smaller offset voltage and the larger chip size should be considered.

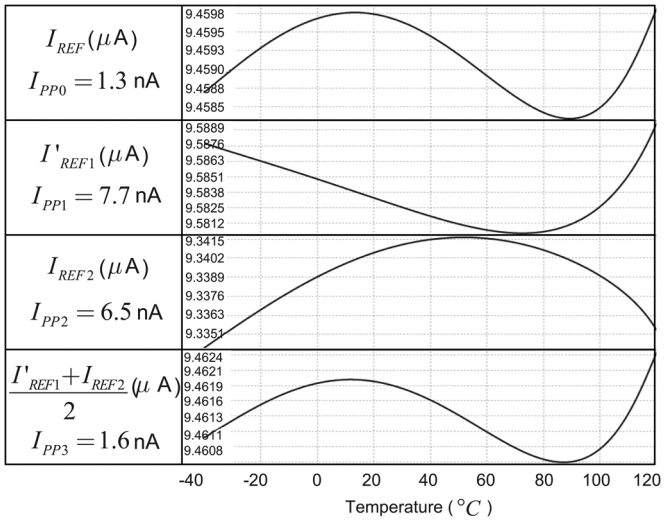

Fig. 9. Simulated proposed BGR circuit in the varying temperature from -40 °C to 120 °C with a supply voltage of 1.2 V and a typical CMOS process.

IV. Simulation and Measurement Results

Fig. 9 presents the simulated results of the reference currents in the proposed BGR circuit. The temperature dependence of the resistors is not considered in this analysis, which uses ideal resistors, since all resistors in the proposed BGR circuit are the same type, and the variations in the two resistors are the ratio in the numerator and denominator, as presented in (26). Reference current I_{REF} is approximately 9.46 μA and its peak-to-peak current I_{PP0} is 1.3 nA (1 ppm/°C) over a wide temperature range of -40 to 120 °C. In BGR core A, passing a current-mirror circuit gives the reference current, I'_{REF1}, a well balanced curvature-up characteristic. It is approximately 9.59 μA, and its peak-to-peak current I_{PP1} is 7.7 nA. In BGR core B, using the conventional structure, the reference current, I_{REF2}, has a well balanced curvature-down characteristic. It is around 9.34 μA, and its peak-to-peak current I_{PP2} is 6.5 nA. The half summing current, $(I'_{REF1}+I_{REF2})/2$, shows the same current level as the proposed reference current I_{REF}, and it also shows similar curvature characteristics to I_{REF}. However, the ideal current summing shows a peak-to-peak current of 1.6 nA, since a difference exists between the real current summing circuit and the ideal current summing. We can see that the proposed curvature-compensated technique increases by approximately 5 to 6 times for the precision of reference currents compared with the BGR cores A and B.

Fig. 10 shows the chip micrograph and the layout of the proposed BGR circuit, which is fabricated in a standard 0.13-μm CMOS process and the total chip size is approximately 0.063 mm^2 (275 μm $\times$ 230 μm). The package is a 64-pin thin-quad-flat-pack (TQFP). In order to reduce the process mismatch effect, the common-centroid technique is used for the layout of BJTs and the active MOS transistors, where 1 BJT of Q1 is symmetrically surrounded by the 8 BJTs of Q0, and 1 BJT of Q3 is symmetrically surrounded by the 8 BJTs of Q2. In addition, extra dummy BJTs and MOS transistors are adopted to achieve better matching for BJTs and the active MOS transistors.

Since the BGR circuit is highly sensitive to the CMOS process, the variation in resistance may significantly affect the accuracy of the output reference voltage. In general, a trimming circuit is required to obtain the best results; however, this significantly increases the circuit complexity, the chip area, and the cost. This study does not use any trimming circuits and the unit resistance of R_u, around 9.67 kΩ, is chosen for better matching to achieve higher precision, as mentioned in Table I. $R0$ and $R4$ have the same resistances of 14.51 kΩ (9.67 kΩ + 9.67 kΩ||9.67 kΩ) and all resistors are generated by series connection and parallel connection of the unit resistors.

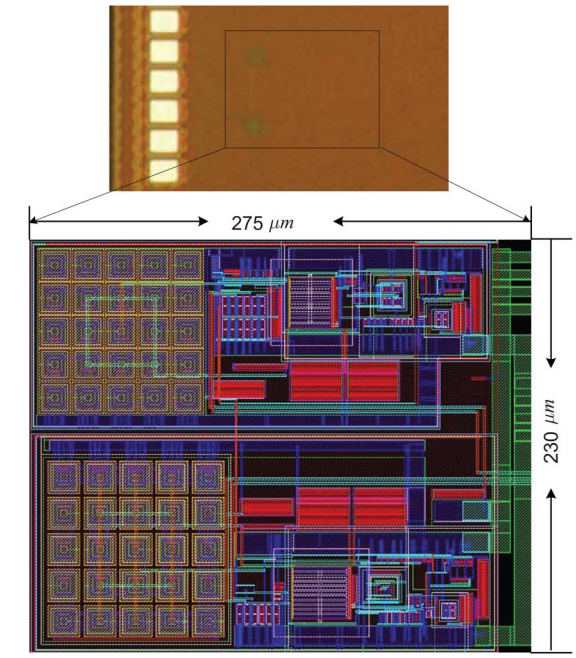

Fig. 10. The chip micrograph and layout of the proposed BGR circuit (275 μm $\times$ 230 μm).

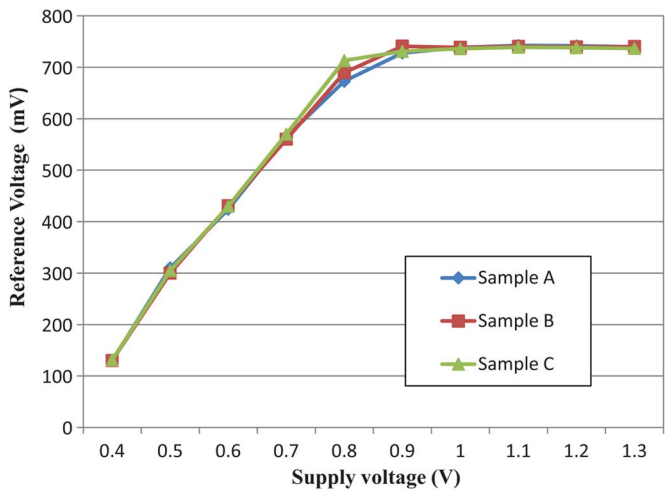

Fig. 11. Measured reference voltage versus supply voltage at room temperature.

Fig. 11 demonstrates the measured reference voltages of 3 samples versus the power supply voltage at room temperature. We can see that the BGR circuit can properly operate when the supply voltage is higher than 1 V. Fig. 12 presents the measured reference voltages as a function of temperature at different supply voltages. In the temperature range of -40 to 120 °C, TCs are 4.2 ppm/°C at the supply voltage of 1.2 V, 9.5 ppm/°C at the supply voltage of 1.15 V, and 9.3 ppm/°C at the supply voltage of 1.25 V.

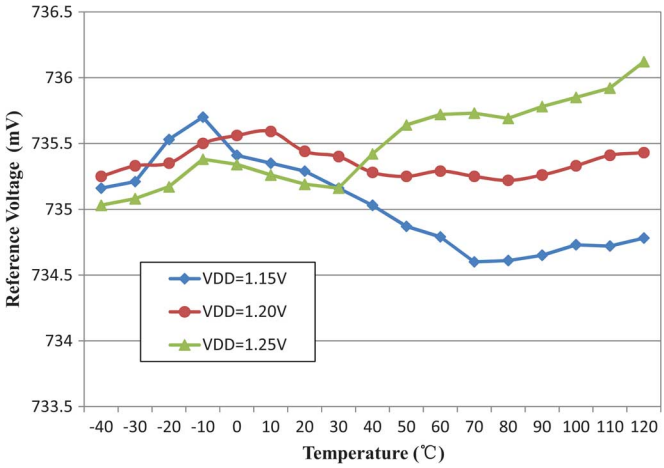

Fig. 12. Measured temperature dependence for different supply voltages.

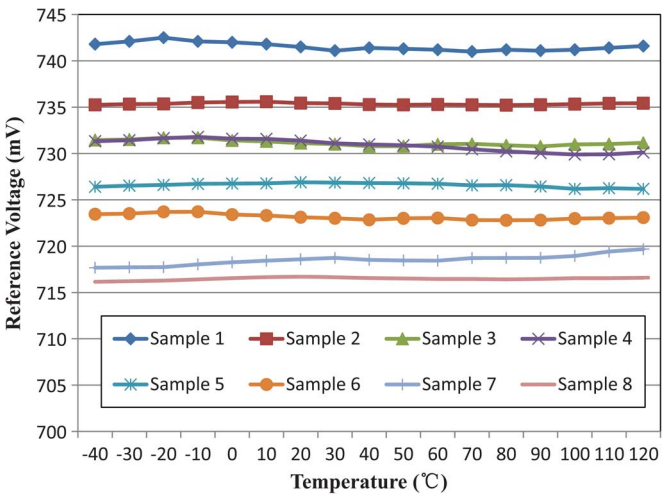

Fig. 13. Measured temperature dependence for 8 different samples at a supply voltage of 1.2 V.

Fig. 13 shows the measured temperature dependence of the proposed reference voltages for 8 random samples at the supply voltage of 1.2 V. All samples show stable reference voltages versus temperature from 717 mV to 743 mV. The random offsets would be the major source of voltage shift, as was simulated in Table II. Table III summarizes the performances, where a TC as low as 4.2-ppm/°C is achieved with an approximately 500-μV peak-to-peak voltage. Without any trimming circuits, the proposed BGR circuit from 8 random samples shows an average TC of 9.3 ppm/°C, which is an extremely efficient value. In addition, we can see that most of the samples have TCs around 8 ppm/°C.

The measured results show larger voltage variations than the simulated results, since the BGR circuit is an extremely sensitive block. As discussed in previous parts, many error sources exist, such as random offset, mismatch between BJTs, mismatch of current mirrors, and mismatch among resistors. All of these can impact the accuracy of the reference voltage. In addition, there are random noise sources (flicker noise, thermal noise, and other surrounding noise), and they also cause error in the reference voltage [21], [22]. The measured errors (the difference between the reference voltage and the average reference voltage) over time for three samples are shown in Fig. 14. The

TABLE III
MEASUREMENT OF 8 DIFFERENT SAMPLES FROM −40 TO 120 °C AT SUPPLY VOLTAGE OF 1.2 V

Sample	TC without trimming (ppm/°C)
1	10.1
2	4.2
3	8.1
4	15.4
5	6.2
6	7.9
7	17.4
8	4.8

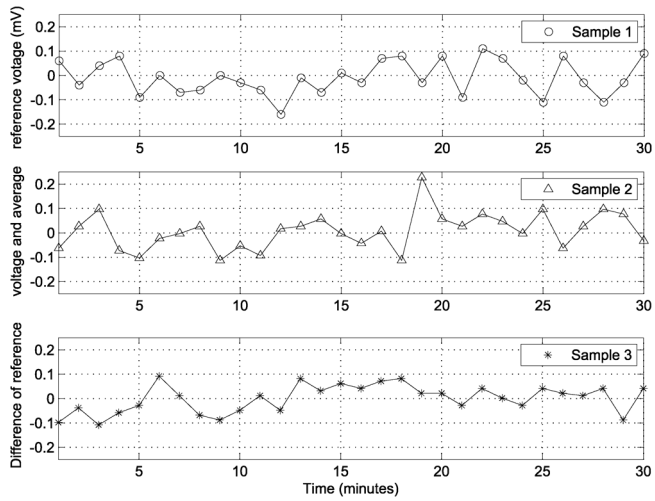

Fig. 14. Measured output reference voltage over time at room temperature.

average peak-to-peak noise is approximately 200 μV, which is much smaller than the best measured peak-to-peak voltage of approximately 500 μV (4.2 ppm/°C) and the average measured peak-to-peak voltage of approximately 1100 μV (9.3 ppm/°C).

In frequencies of 100 Hz to 100 kHz, the proposed BGR circuit without any trimming blocks shows a measured PSRR of −30 dB. Table IV shows a comparison with the results from other studies, and we can see that the present study (without the trimming circuits) obtains the best average TC of 9.3 ppm/°C and a TC as low as 4.2 ppm/°C due to the proposed efficient compensation technique. Compared to the circuit in [5], the proposed BGR circuit consumes more current because of the feedback loop components. The two opamps use more current in order to increase the loop bandwidth for the improved high-frequency PSRR. By using more current for the opamps, the proposed BGR circuit achieves a PSRR of −30 dB at 100 kHz, while the PSRR in [5] is −25.5 dB.

V. CONCLUSION

A high-precision BGR circuit with a low supply voltage is presented in this study. The proposed curvature-up technique and the conventional structure with curvature-down characteristic are used to achieve a high-accuracy reference voltages. The proposed BGR circuit without any trimming circuits shows a measured TC as low as 4.2 ppm/°C over a wide temperature range of 160 °C (−40 ∼ 120 °C) at a power supply voltage of 1.2 V. For 8 random samples, the average TC is approximately 9.3 ppm/°C, which is the best performance compared with other published results. The total current is approximately 120 μA at the room temperature. A measured PSRR of −30 dB is achieved at a frequency range from 100 Hz to 100 kHz.

TABLE IV
COMPARISON WITH OTHER PUBLISHED RESULTS

Parameter	This work	Ref.[1] [2011]	Ref.[2] [2012]	Ref.[5] [2006]	Ref.[10] [2014]	Ref.[18] [2013]
Supply Voltage (V)	1.2	1.2	2.5	1.0	1.2	0.7/1.2
Current Consumption (μA)	120	40	38	50	36	52.5/100 (nW)
Ref. Voltage (mV)	735	487.6	617.7	540	767	548/1090
Temp. Range (°C)	$-40\sim120$	$-40\sim110$	$-15\sim150$	$0\sim100$	$-40\sim110$	$-40\sim120$
Simulated TC (ppm/°C)	1.0	—	—	7.5	—	—
Best TC (ppm/°C) (untrimmed)	4.2	8.9	3.9	13.4	11.5	—
Average TC (ppm/°C) (untrimmed)	9.3	11.8	15.6	13.4	15.9	114/147
Number of samples	8	5	5	1	8	9
PSRR (dB)	-30 @100kHz	-16 @100kHz	—	-25.5 @10kHz	-37 @100kHz	$-56/-62$ @100Hz/100Hz
Chip Area (mm^2)	0.063	0.1	0.102	0.11	0.036	0.025/0.03
CMOS Process (μm)	0.13	0.5	0.35	0.25	0.18	0.18

The total chip size is approximately 0.063 mm^2 in a standard 0.13-μm CMOS process.

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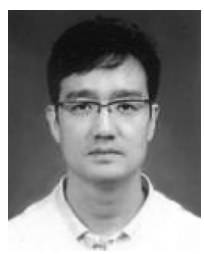

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