A Comprehensive Signature Analysis Scheme for Oscillation-Test

Jeongjin Roh and Jacob A. Abraham, *Fellow, IEEE*

***Abstract*—A low-cost and comprehensive built-in self-test (BIST) methodology for analog and mixed-signal circuits is described. We implement a time-division multiplexing (TDM) comparator to analyze the response of a circuit under test with minimum hardware overhead. The TDM comparator scheme is an effective signature analyzer for on-chip analog response compaction and pass/fail decision. We apply this scheme to an oscillation-test environment and implement a low-cost and comprehensive vectorless BIST methodology for high fault and yield coverage. Our scheme allows a tolerance in the output response, a feature necessary for analog circuits. Both oscillation frequency and oscillation amplitude are measured indirectly to increase the fault coverage. We provide a theoretical analysis of the oscillation that explains why the amplitude measurement is essential. Simulation results demonstrate that the proposed scheme can significantly reduce test time of the oscillation-test while achieving higher fault coverage.**

***Index Terms*—Built-in self-test (BIST), design for test, mixed-signal test, oscillation test, singature analysis.**

I. Introduction

ANALOG circuit testing has been considered to be difficult and complicated, since the specification for a correct output can only be described within a tolerance margin. Moreover, the input waveform may not be exactly the same as the ideal input waveform due to noise and tolerance specifications of the circuit that produces the waveform. The response of the circuit under test (CUT) will, therefore, be imprecise because of the imprecise input signal. Tolerances in the component values of the analog circuit can also cause the response of the circuit to be different from the ideal response. The problem of analog circuit testing has been made more difficult by the trend of integrating analog circuits with digital blocks, and by the reduction of access ports for analog circuits in these mixed-signal circuits. Thus, mixed-signal testers with demanding requirements of speed, accuracy, memory storage, and low noise are very expensive.

Built-in self test (BIST) is considered to be a promising solution to the increasing complexity of these test problems. The two major objectives of BIST are to decrease the amount of testing time and to reduce the difficulties of analog test for complex mixed-signal circuits. In addition, BIST can be a solution to testing the intellectual property (IP), core-based system-on-a-chip (SOC) ICs. In most cases, the core integrators have limited knowledge of the internal circuit design and operation of IP cores. Therefore, the core creator must prepare the testability solution and deliver it with the IP core.

In order to have a comprehensive BIST solution for all these problems, the test stimulus generator, measurement circuit, and pass/fail decision circuit need to be placed on the same chip. Then, the BIST can be used not only for manufacturing test, but also for field test and as a solution for IP core test.

Several BIST schemes have been proposed in the past for testing analog and mixed-signal circuits [1]–[6]. Some of them [1], [2] have focused on on-chip test stimulus generation. Even though various schemes for on-chip sinusoidal or multitone stimulus generation have been developed, hardware overheads for these schemes may still be unacceptable for many mixed-signal circuits. Other work focused on efficient on-chip measurement and decision schemes [3]–[6]. Many schemes assume the availability of on-chip hardware such as linear feedback shift registers (LFSRs) [3], [4], an analog–digital converter (ADC) [3], [5], [6] or a digital–analog converter (DAC) [3]. In some research, powerful computing capability such as a DSP core is assumed to be available on-chip even for mixed-signal circuits [3].

The issue of circuit specification tolerance margins is covered well in [5] and [6], but these schemes assume an on-chip ADC, which makes them limited to only certain mixed-signal circuits. Test-stimulus generation is another unsolved problem for these schemes.

Tolerance margin can be addressed as an issue in fault classification. Generating a boundary between good and faulty circuits is not simple in the analog domain, and has been considered a difficult problem. There are two reasons for this problem. First, many proposed techniques are defect-oriented tests, and the direct measurements of specifications are avoided. The go/no-go decision of the test has to be made from the indirect measurements of the specifications. Second, unlike in digital circuits, the boundary of analog circuits should include the tolerance margins. A solution to this problem could be the application of statistical techniques [3], [7]–[10]. For thousands of samples in the training set, several statistical techniques have been applied to classify the faulty circuits from good circuits. These statistical techniques can also be applied to the output response of our TDM comparator to further increase the fault coverage, but it is beyond the scope of this paper.

The oscillation-test methodology (OTM) [11], [13]–[21] has been proposed as a vectorless scheme for both general manufac-

Manuscript received February 25, 2002; revised December 1, 2002. This work was supported in part by the National Science Foundation under Grant CCR-9731433 and in part by Subcontract SA3271JB from the University of California Berkeley under Prime Contract 98-DT-660 from Microelectronic Advanced Research Corporation. This paper was recommended by Associate Editor R. C. Aitken.

J. Roh is currently with the Department of Electrical Engineering, Hanyang University, Ansan 426-791, Korea (e-mail: jroh@hanyang.ac.kr).

J. A. Abraham is with the Department of Electrical and Computer Engineering, University of Texas, Austin, TX 78712 USA (e-mail: jaa@cerc.utexas.edu).

Digital Object Identifier 10.1109/TCAD.2003.818133

turing test for defects using external testers and an oscillation BIST (OBIST) scheme. This vectorless testing concept is appealing since the generation of an on-chip pure sinusoidal stimulus requires significant hardware overhead. Therefore, OTM seems to be a promising solution for the test stimulus problem. Most research on OTM has focused on how to convert a circuit into an oscillator in test mode. However, there has not been extensive research on: 1) how to maximize the fault coverage and 2) how to minimize the test time [22]. We describe an efficient signature analysis scheme for these two important issues.

In this paper, analog filters are used as our benchmark circuits following the usual practice [11]–[14], [18]–[21]. However, there will be no limitation in applying our technique to other benchmark circuits. For example, our technique can be applied to the oscillation signal from the dual-slope ADC [11]. Our technique will analyze the oscillation output from the dual-slope ADC when it is converted into a oscillator in test mode. The nominal oscillation frequency of the dual-slope ADC was 1.53 MHz in [11], and our TDM comparator can be used to measure the frequency and amplitude as is done in this paper.

The only exception would be the digital-to-analog converter (DAC) test in [17] in which the DAC under test is located in the feedback loop of a single bit delta-sigma modulator. To establish different oscillation conditions, the DAC input is switched between two predetermined digital codes stored in two test registers. The quality of the DAC is measured by quantifying the modulator output. Even though this paper has been published as an oscillation-test, it is significantly different from other oscillation-test methodologies in the sense that the oscillation is controlled by the digital input to the DAC under test, unlike other methods that move the poles into the right-hand plane in the s-domain. That is, the DAC under test in this approach controls the oscillation by digital input to the DAC, and requires relatively large hardware overhead, while the traditional oscillation-test boasts its simplicity. Therefore, in our opinion, Hassan's technique [17] may not be categorized as a general oscillation-test.

This paper is organized as follows. Section II addresses the two issues in detail. Section III explains the TDM comparator scheme and how we can implement a comprehensive BIST scheme by incorporating the oscillation-test mode. We describe a detailed implementation of the signature analyzer, and also review the advantages of the proposed scheme. The nonlinear analysis of oscillation behavior is done in Section IV. Section V gives the simulation results for catastrophic faults as well as parametric faults to illustrate the effectiveness of the proposed technique. Conclusions are presented in Section VI.

II. Oscillation Test Methodology

The basic idea of OTM is to convert a CUT into a circuit that oscillates. Faults in the CUT which cause the oscillation frequency to deviate from its tolerance band can be detected. When this technique is used, no application of test vectors is necessary.

There has been significant research on the oscillation-test methodology. However, in spite of the importance of the two issues of test time and fault coverage, which would significantly affect the quality of the test, these issues have not been thoroughly addressed in prior work. Most previous research has focused only on how to convert a CUT to an oscillator; a method for analyzing the oscillation frequency on-chip has not been thoroughly developed. In this paper, we are focusing on these two important issues of testing, which are fault coverage and test time.

A. Fault Coverage

Many researchers have shown that the OTM can achieve high fault coverage for catastrophic faults. However, there is a limitation on the maximum parametric fault coverage that can be achieved by measuring the oscillation frequency. Recent research [19] shows that the oscillation frequency cannot achieve sufficiently high fault and yield coverage, and it proposes to measure the amplitude of the oscillation as well as the oscillation frequency. It has demonstrated that some of the parametric faults do not affect the oscillation frequency, while they change the oscillation amplitude. Therefore, in order to achieve high parametric fault coverage, it would be essential to detect the variation of both oscillation amplitude and oscillation frequency.

In [19], the oscillation amplitude was measured only at the primary output of the CUT, and an on-chip amplitude measurement technique was not developed. The oscillation amplitude at the primary output of the circuit could be sensitive only to the faulty components adjacent to it. The oscillation amplitude may not be sensitive to the faulty components that are not adjacent to the primary output. In order to achieve high parametric fault coverage, internal nodes should be monitored in addition to the primary output. This approach will be developed in this paper. In our simulations in Section V, it will be shown that the monitoring of internal nodes can significantly increase the fault coverage.

B. Test Time to Measure Oscillation Frequency

Significant test time can be another drawback of the oscillation-test methodology, since the accurate calculation of oscillation frequency requires a large measurement time. The test time of oscillation-test would be on the order of seconds if we do not incorporate an efficient signature analysis technique, as we show in Section V. Direct measurement of the oscillation frequency could take a second or more. Even worse, if a large circuit is partitioned into several small circuits that oscillate [19], the total test time using oscillation-test could be more than several seconds, which is prohibitively long for a go/no-go test in production.

Also, it has been found that different oscillator structures have different sensitivity to a set of components, and it has been suggested that it would be desirable to construct more than one oscillator from the CUT to increase the fault coverage [16]. This will increase the test time even further.

In this paper, we demonstrate that the test time can be significantly reduced by indirectly measuring the oscillation frequency. Direct measurement of the low-frequency oscillation signal takes significant test time. By using the fast comparator as a signature analyzer, we can measure the oscillation frequency with high accuracy. Our TDM comparator scheme will be shown to be an effective technique to measure both the oscillation frequency and the amplitude of the oscillation signal with significantly less test time.

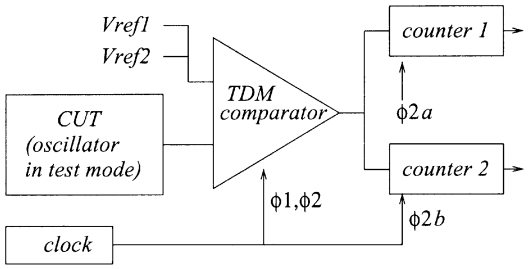


Fig. 1. Comprehensive BIST scheme.

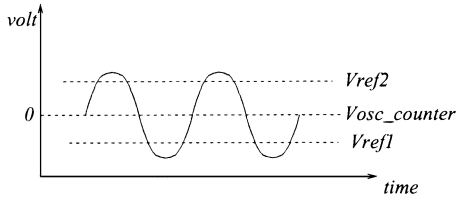


Fig. 2. Example of an oscillation signal with reference voltages.

III. TDM Comparator BIST Scheme

Fig. 1 shows the comprehensive BIST scheme using the TDM comparator. The CUT is converted to an oscillator in test mode [11], then, the oscillation waveform is compared with the reference voltages 1 and 2, and the comparison results are accumulated into the counters according to the clocks $\phi 1$ and $\phi 2$, using time-division multiplexing. The tolerance to noise is increased by accumulating the comparator output sequence, since the effect from the noise and jitter can be canceled out as was done in the integrator scheme [5]. Also, the accumulation generates a compressed signature, so that the storage requirements for the BIST circuit can be relieved. In general, the proposed scheme generates effective signatures with only one cycle of the oscillation signal after the oscillation has stabilized. However, the measurement could be repeated for several cycles and results could be averaged to increase the tolerance to noise even more. In the simulation results in Section V, only one cycle of oscillation is measured.

Each counter has a unique value as a signature for the CUT, and the respective tolerance band is decided as shown in Section V. Reference voltages can be determined during the BIST design phase allowing a designer more flexibility to analyze the output response. Fig. 2 shows an example of two reference voltages. When the oscillation signal is higher than a reference voltage, the comparator will generate a sequence of ones for each TDM clock cycle. In this case, we are assuming that the oscillation signal is connected to the positive input and the reference voltage is connected to the negative input of the TDM comparator. In Fig. 2, for example, V_{ref1} will have a long sequence of ones since the voltage level of the oscillation signal is higher than V_{ref1}, while V_{ref2} will have a short sequence of ones at the TDM comparator output. The reference voltage of $V_{osc\_counter}$ is the virtual ground of analog circuits, which is $Vcc/2$ in general. Detailed explanations follow.

A. Low-Cost TDM Comparator Design

Fig. 3 shows a popular comparator circuit, which was first used to implement a six-bit flash ADC [32] in 1979. When the half-clock cycle $\phi 2$ turns on, the switch connecting the input and output of the inverter is turned on and the inverter is set to its bistable operating point, V_B, where the output voltage equals the input voltage

$$V_{\mathrm{out}} = V_x = V_B \approx \frac{V_{\mathrm{dd}} + V_{\mathrm{ss}}}{2}. \tag{1}$$

With this inverter set to its bistable operating voltage, the other side of C is charged to V_{ref}

$$V_y = V_{\mathrm{ref}} \tag{2}$$

$$V_c = V_y - V_B = V_{\mathrm{ref}} - V_B. \tag{3}$$

When the $\phi 2$ clock turns off, the inverter is put into a very unstable condition and will go either high or low depending on its input voltage. When the $\phi 1$ clock turns on, the other side of C is pulled to V_{in}. Since the inverter side of the capacitor is floating, C must keep its original charge, and the inverter's input will change by the voltage difference $V_{\mathrm{in}} - V_{\mathrm{ref}}$. Since the inverter's input was bistable, the voltage difference will determine whether the output will become low or high

$$V_y = V_{\mathrm{in}} \tag{4}$$

$$V_x = V_{\mathrm{in}} - V_c = V_{\mathrm{in}} - (V_{\mathrm{ref}} - V_B) \tag{5}$$

$$V_{\mathrm{out}} = V_B + A_{v1}(V_x - V_B) \tag{6}$$

$$= V_B + A_{v1}(V_{\mathrm{in}} - V_{\mathrm{ref}} + V_B - V_B) \tag{7}$$

$$= V_B + A_{v1}(V_{\mathrm{in}} - V_{\mathrm{ref}}). \tag{8}$$

A_{v1} is the gain of an inverter as shown in (9), which is actually the gain of a push-pull CMOS inverting amplifier where g_{m1} and g_{m2} are the small-signal transconductances from gate to channel for n-channel and p-channel transistors, respectively [34]. Also, g_{ds1} and g_{ds2} are conductances of the drain-to-source for n-channel and p-channel transistors, respectively. Since g_m is significantly larger than g_{ds}, a CMOS inverter can have sufficient gain as an amplifier

$$A_{v1} = -\frac{g_{m1} + g_{m2}}{g_{\mathrm{ds1}} + g_{\mathrm{ds2}}}. \tag{9}$$

The comparator in Fig. 3 is modified to implement the TDM comparator in Fig. 4. Two comparator stages are shown in Fig. 4. The first stage is a modified version of the comparator in Fig. 3, and the second stage is a simple inverting comparator [34] to

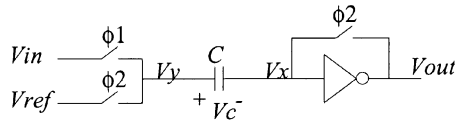


Fig. 3. Low-cost CMOS comparator.

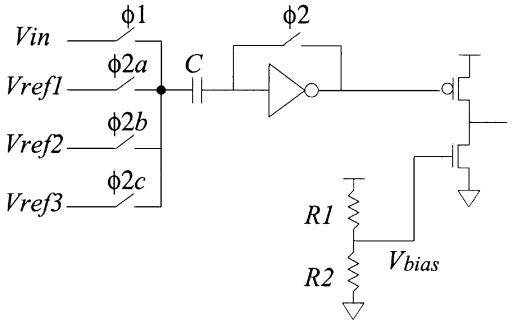


Fig. 4. TDM comparator.

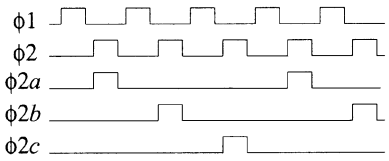


Fig. 5. Clocks for the TDM comparator.

convert the output level of the first stage into two binary levels. Since the output of the first-stage comparator during $\phi 2$ is an undesirable intermediate level, approximately $(V_{\rm dd} + V_{\rm ss})/2$, it must be converted to binary levels for digital counters. The bias voltage, $V_{\rm bias}$, for the second comparator does not require high precision, so voltage division by resistors is used here. The trip voltage $V_{\rm trip}$ of the second comparator depends on $V_{\rm bias}$, and is easily calculated as in [34]. $V_{\rm trip}$ can be set lower than the $(V_{\rm dd} + V_{\rm ss})/2$, so that the output of the TDM comparator during $\phi 2$ will be zero.

Equation (10) shows the gain of the second comparator, which will increase the overall gain of the TDM comparator in Fig. 4, as shown in (11)

$$A_{v2} = -\frac{g_{m2}}{g_{\rm ds1} + g_{\rm ds2}} \tag{10}$$

$$A_v = A_{v1}A_{v2} = \left[\frac{g_{m1} + g_{m2}}{g_{\rm ds1} + g_{\rm ds2}}\right]\left[\frac{g_{m2}}{g_{\rm ds1} + g_{\rm ds2}}\right]. \tag{11}$$

Fig. 5 shows an example of clocks $\phi 1$ and $\phi 2$ which are common nonoverlapping clocks in digital logic. The switches used here can be implemented with CMOS switches [34]. In Figs. 4 and 5, $\phi 2$ is divided into three clocks, $\phi 2a$, $\phi 2b$, and $\phi 2c$. These three clocks are used to turn on, or *multiplex*, the switches for the three reference voltages, $V_{\rm ref1}$, $V_{\rm ref2}$, and $V_{\rm ref3}$, respectively. Since the reference voltages are multiplexed according to the time slots, $V_{\rm in}$ will be compared with three reference voltages.

B. Voltage Reference Circuit

Accurate voltage reference would be essential for the comparator to generate the correct sequence of ones and zeros for the counters. In general, most analog and mixed-signal circuits have on-chip bandgap reference [33], which generates supply-independent and temperature-independent voltage reference. In CMOS process, the base-emitter voltage of the parasitic bipolar transistor is used to generate the negative temperature coefficient (TC). This negative TC voltage is compensated by the positive TC voltage generation circuit, which is the difference between the base-emitter voltages of two bipolar transistors. Since we are assuming that the bandgap circuit is an existing analog component and is not part of BIST, the detailed discussion of the bandgap circuit design is referred to general textbooks such as [34].

The TDM comparator can use the same on-chip bandgap reference as other analog circuits, or can use the external voltage reference in test mode. Fig. 6 shows an example of the voltage division circuit, which is commonly used in many precision analog circuits such as analog-to-digital converters. The hardware overhead will be one amplifier and n resistors where n is the number of voltage references for the TDM comparator. The input voltage $V_{\rm in}$ comes either from the on-chip bandgap reference or from the external voltage reference as mentioned above. It can easily be shown that the voltage references can be represented as

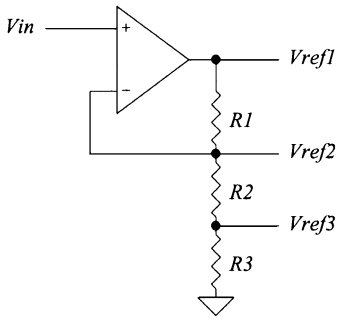


Fig. 6. Example of a voltage reference circuit.

$$V_{\rm ref1} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} \times V_{\rm in} \tag{12}$$

$$V_{\rm ref2} = V_{\rm in} \tag{13}$$

$$V_{\rm ref3} = \frac{R_3}{R_2 + R_3} \times V_{\rm in}. \tag{14}$$

The process variation of resistors and capacitors can be as much as 10% or higher in standard CMOS processes. However, this voltage reference circuit is a pure resistive circuit, and the process variation has an insignificant effect on accuracy. Process variations will affect the sheet resistance of the resistive layers such as a salicide-blocked polysilicon. The variation of sheet resistance will increase or decrease resistance of all resistors in the circuit. For example, even if we assume that the sheet resistance has 10% variation from the nominal value, the voltage references in Fig. 6 can still maintain the same accurate voltage levels regardless of the process variation. It can be simply proved from (12) or (14), as the resistors in the numerator have 10% variation, while the resistors in the denominator also have 10% variation. Since both numerator and denominator have the same variation, the reference voltage level does not change. In other words, the ratio of components is more important than the absolute value of components. For most analog circuits, the ratio of the components in the local area will determine the performance, since all components will be placed closely in the layout. Therefore, the primary interest is in matching properties of local components, and the intradie variation of components will not be a significant factor.

However, the mismatches of each resistor would degrade the accuracy of the voltage references. The common analog layout practices such as the interdigitization and common-centroid would be required to guarantee process-independent voltage references. If there is an error in the reference circuit, the TDM comparator's output will be significantly different from the nominal value, and can be easily detected.

C. Measurement of Both Oscillation Frequency and Amplitude

The signature analysis of oscillation-test methodology should consider that the oscillation signals of most analog circuits are low-frequency signals. For example, the oscillation frequencies of the state variable filter in Section V and dual-tone multifrequency in [19] are around 1 kHz. If we try to measure the oscillation frequency directly, it may take a significant amount of

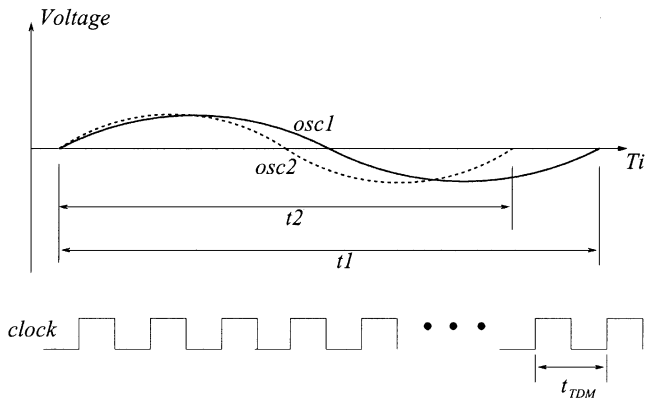


Fig. 7. Detection of the difference of two oscillation signals.

time, which will increase the manufacturing cost. Therefore, it is preferable to have an indirect measurement scheme of oscillation frequency and amplitude, which can also represent the tolerance band of the CUT.

The TDM comparator scheme measures the width and amplitude of the oscillation by comparing the oscillation signal with each reference voltage for each time slot. This scheme is an indirect and efficient measurement of both oscillation frequency and amplitude with low hardware overhead. Since the digital clock is significantly faster than the oscillation frequency, multiplexing the clocks $\phi 1$ and $\phi 2$ will have a sufficient number of comparisons for each oscillation cycle. The comparison result will be accumulated into the digital counters which represent the signature of the CUT.

The oscillation frequency, $f_{\rm osc}$, can be calculated from the TDM counter value as

$$f_{\rm osc} = \frac{f_{\rm TDM} \times N_{\rm cycles}}{osc\_counter} \tag{15}$$

$N_{\rm cycles}$ is the number of oscillation cycles that the TDM comparator has operated on, and $osc\_counter$ is the total number of clocks during $N_{\rm cycles}$. $f_{\rm TDM}$ is the clock frequency for the TDM clock, and it can be represented as

$$f_{\rm TDM} = \frac{f_s}{N_{\rm TDM}} \tag{16}$$

where $N_{\rm TDM}$ is the number of time-division multiplexing and f_s is the frequency of the main system clock.

When we use the TDM comparator to measure the oscillation frequency, a separate counter, $osc\_counter$, has been dedicated to count all clocks in the oscillation cycles. The reference voltage for $osc\_counter$ is 0 volt, which is the analog ac ground as shown in Fig. 2. The TDM comparator will detect the beginning and the end of one cycle, and the $osc\_counter$ will count all the clocks within that cycle.

The required minimum TDM clock frequency to detect the deviation of oscillation frequency can be calculated by the nominal oscillation frequency of the CUT and the required measurement accuracy. For example, Fig. 7 shows two oscillation signals. In order to guarantee the detection of the frequency deviation, at least one more comparison should be done for the osc1 signal. This requirement is summarized in (17), where $t_{\rm TDM}$ is the one clock period and t_1 and t_2 are cycle times of oscillation signal 1 and 2, respectively

$$t_{\rm TDM} < t_1 - t_2. \tag{17}$$

Since the cycle time equals the inverse of the oscillation frequency, (17) can be modified as (18), where $f_{\rm TDM}$ is the TDM clock frequency, and f_1 and f_2 are the frequency of $osc1$ and $osc2$, respectively

$$f_{\rm TDM} > \frac{f_1 \times f_2}{f_2 - f_1}. \tag{18}$$

If the measurement resolution of 1 Hz is desired for the oscillation frequency, then the minimum requirement for the TDM clock speed can be simplified as (19), where the frequency of oscillation signal 2 is substituted by $f_2 = f_1 + 1$

$$f_{\rm TDM} > f_1 \times f_2 \approx f_1^2. \tag{19}$$

From (19), the minimum TDM clock will be 1 MHz if the nominal oscillation frequency is 1 kHz. If the number of time-division multiplexing is three, the system clock frequency of 3 MHz would be sufficient to achieve the accurate measurement of oscillation frequency with 1 Hz measurement resolution.

D. Internal Node Selection to Enhance Testability

The testability of the circuit can be enhanced by observing internal nodes as well as the primary output. The TDM comparator can be modified to observe internal nodes. In Figs. 4 and 5, only the $\phi 2$ clock was divided into three time slots and multiplexed to select the reference voltages, and the output response $V_{\rm in}$ was connected only from the primary output of the CUT.

The $\phi 1$ clock can also be divided into three time slots and multiplexed to select internal nodes of the CUT. Only two additional switches are required to modify the TDM comparator in Fig. 4. The signal from each internal node is compared with its respective reference voltage and is accumulated into its respective counter to generate a signature as shown in Section V.

In the oscillation-test methodology, the sensitivity of the oscillation amplitude is highest for the component that is near the node. If we assume that a resistor is connected to the input node and that the resistor has a parametric fault, then the oscillation amplitude of the input node is more sensitive than the output node. This is shown in the simulations in Section V. This sensitivity gives us significant information, which helps us detect a faulty component. Measuring the output oscillation amplitude alone does not provide sufficient high parametric fault coverage, and monitoring internal nodes can significantly enhance the testability.

In this paper, the selection of internal nodes is achieved through the following steps:

1) indirectly measure the oscillation frequency using a TDM counter, as can be done using (15). Most catastrophic faults and many parametric faults can be detected with this indirect frequency measurement;
2) find the undetected parametric faulty components;
3) monitor internal nodes near the undetected faulty components.

Indirect measurement of oscillation frequency using (15) is only for testability analysis, and the pass/fail decision can be made directly from the $osc\_counter$ value.

Since all transistors have parasitic capacitances, switches of the TDM comparator add parasitic components to the CUT. For example, the node 1 in Fig. 16 is monitored in Section V, so the node 1, which is the negative input of the opamp 1, will have an extra parasitic capacitance caused by a TDM switch. If we ignore the parasitic capacitances of the resistors that would be smaller than the parasitics of the transistors, the total parasitics of the node 1 will be

$$C_{p,\text{total}} = C_{\text{gs},M3} + C_{\text{gd},M3} + C_{\text{gb},M3} + C_{\text{gs,TDMswitch}}. \tag{20}$$

$M3$ is an input transistor of the opamp in Fig. 17, which is used for the state variable filter. The gate-to-source capacitance C_{gs} is the dominant one when a transistor is in saturation mode, whereas the gate-to-drain capacitance C_{gd} and the gate-to-bulk capacitance C_{gb} are relatively small [34]. In general, the lengths of the opamp transistors are at least twice the minimum to decrease the channel-length modulation effect, while the lengths of CMOS switches are minimum to reduce the turn-on resistance. Also, the input transistor pair of the opamp has a large width in order to increase the gain and to decrease the $1/f$ noise. Therefore, the parasitics of the large input pair would be more significant than the parasitics of the switches when all transistors are in saturation mode. When the CUT is in normal operation mode, the BIST circuit is disabled, which means that the switches of the TDM comparator are in the off state. When the transistors turn off, C_{gs} decreases significantly. Since the TDM switches turn off in normal operation mode and turn on only in test mode, $C_{\text{gs,TDMswitch}}$ in the off state will be even further reduced and will become less significant than $C_{\text{gs},M3}$. In summary, $C_{\text{gs},M3}$ is the dominant parasitic capacitance and the parasitic capacitance of the TDM switch is insignificant. Similar reasoning can be applied to other internal nodes. A further discussion of parasitic capacitance can be found in [34].

E. Virtual Ground Explosion

In this section, an interesting circuit behavior during the oscillation will be investigated, which will be used by the TDM comparator to increase the fault coverage. Fig. 8 shows an analog integrator, which is a basic analog building block and also a part of our benchmark circuit, the state variable filer, in Section V-A

$$V_{\text{out}}(t) - V_x(t) = \frac{1}{\text{RC}} \times \int [V_{\text{in}}(t) - V_x(t)]\, dt. \tag{21}$$

Equation (21) shows the well known integrator equation from Fig. 8. Because of the high gain of the opamp, the negative input $V_x(t)$ can be treated as a virtual ground. In the ideal case, the integrator output will follow (21), and design effort has to be made to limit the signal swing so that the deviation from the ideal equation can be minimized.

The practical opamp will always have the maximum output swing, which is decided by the power supply rails and the architecture of the opamp's output stage. During oscillation, the signal swing can be out of the operation range, and the signal will be clipped by the opamp maximum output swing as shown in Fig. 9.

When clipping of the signal happens, the voltage input to the virtual ground will deviate from the ideal small-signal behavior. In other words, the negative input of the opamp fails to be a virtual ground showing large-signal behavior, which will be called *virtual ground explosion* in this paper. Fig. 9 shows the virtual ground explosion during the output clipping state. This can be observed from circuit simulation as shown in Fig. 18 in our benchmark circuits.

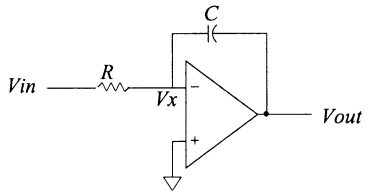


Fig. 8. Integrator.

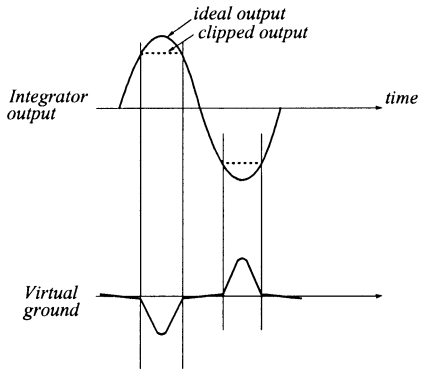


Fig. 9. Virtual ground explosion due to the limited output swing of an operational amplifier.

Most of the previous oscillation-test papers have used the technique to move the poles into the RHP, and let the power supply rails operate as a limiter. In these cases, if we simply try to measure the amplitude at the primary output, the parametric faults will not vary the maximum amplitude, which is the power supply rail, and cannot be detected. Saturation is a usual phenomenon in oscillator design, and a direct measurement of the oscillation amplitude is not possible in most cases. In most oscillation-tests, the feedback circuit is implemented either by an inverter or by a direct feedback connection to minimize hardware overhead [11]–[15], [19], [21]. Therefore, the virtual ground explosion is almost certain to happen in oscillation-test. The theoretical analysis of a nonlinear oscillation behavior is provided in detail in Section IV. It also shows that the automatic gain control (AGC) technique should not be used in OTM, even though the AGC is a common technique in general oscillator design.

Virtual ground explosion is not a necessary condition for applying our technique. However, when it happens, our method can have extra information from it to increase the fault coverage. Without internal node monitoring to observe the virtual ground explosion, it is not easy to measure the amplitude even if we assume a dedicated high-resolution ADC for amplitude measurement. If we only measure the final oscillation output without internal node monitoring, many parametric faults do not vary the amplitude since the amplitude is already clipped to the power supply rails. Thus, maximizing the fault coverage for parametric faults will not be easy without monitoring the internal nodes and observing the virtual ground explosion.

F. Effect of Noise, Jitter, and Clock Synchronization

For analog and mixed-signal circuits, noise and clock jitter are always significant problems that make testing more difficult. Noise and jitter will cause errors in the signatures of CUTs. Also, for the TDM comparator scheme, clock synchronization is another problem that should be addressed since the oscillation starts asynchronously with TDM clock. In this section, we analyze how these problems affect our signature analysis technique.

$$\varepsilon_T(t) = \varepsilon_S(t) + \varepsilon_J(t) + \varepsilon_W(t). \tag{22}$$

Three error sources are shown in (22), where the total error $\varepsilon_T(t)$ is the sum of the clock synchronization error $\varepsilon_S(t)$, clock jitter error $\varepsilon_J(t)$, and white noise $\varepsilon_W(t)$. Flicker noise, which is also called $1/f$ noise, could be another significant noise source in low-frequency region, but it is ignored in our analysis since the white noise is dominant in the high-frequency region.

Let us suppose that the comparison timing for N samples is given by

$$t_i = i \times T_{\mathrm{TDM}} - 0.5T_{\mathrm{TDM}} + S_i + J_i \qquad i = 1, 2, \ldots, N \tag{23}$$

where T_{TDM} is a clock period, S_i is a random variable with uniform distribution representing the clock synchronization error, and J_i is a Gaussian random variable representing the clock jitter. $0.5T_{\mathrm{TDM}}$ is subtracted to show the first comparison will be done after a half clock period. $\varepsilon_S(t)$ and $\varepsilon_J(t)$ can be represented as the errors in oscillation amplitude caused by the sampling time errors as shown as

$$\begin{aligned}\varepsilon_S(t_i) =& V_{\mathrm{osc}}(iT_{\mathrm{TDM}} - 0.5T_{\mathrm{TDM}} + S_i) \\ & - V_{\mathrm{osc}}(iT_{\mathrm{TDM}} - 0.5T_{\mathrm{TDM}})\end{aligned} \tag{24}$$

$$\begin{aligned}\varepsilon_J(t_i) =& V_{\mathrm{osc}}(iT_{\mathrm{TDM}} - 0.5T_{\mathrm{TDM}} + J_i) \\ & - V_{\mathrm{osc}}(iT_{\mathrm{TDM}} - 0.5T_{\mathrm{TDM}}).\end{aligned} \tag{25}$$

Fig. 10 shows the ambiguous interval with the oscillation signal $V_{\mathrm{osc}}(t)$ and the TDM clock. Since the clock is not synchronized with V_{osc}, there is a possibility of inaccurate counting in our technique. The comparison is done at the falling edge of the clock. However, since the clock is not synchronized with V_{osc}, the first falling edge can be varied by ε_S and ε_J, which are shown in Fig. 10 as an ambiguous interval. The uniform and the Gaussian probability density function (pdf) of S_i and J_i are shown below.

$$\mathrm{pdf}(S_i) = \begin{cases} f_{\mathrm{TDM}}, & \frac{-T_{\mathrm{TDM}}}{2} < S_i < +\frac{T_{\mathrm{TDM}}}{2} \\ 0, & \text{otherwise} \end{cases} \tag{26}$$

$$\mathrm{pdf}(J_i) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{x^2}{2\sigma^2}\right]. \tag{27}$$

We will assume that the $V_{\mathrm{osc}}(t) = A \times \sin(2\pi f_{\mathrm{osc}} t)$, where A is the oscillation amplitude and f_{osc} is the oscillation frequency. The sequence of comparator input samples will be

$$V_{\mathrm{osc}}(t_i) = A\sin(2\pi f_{\mathrm{osc}} t_1), A\sin(2\pi f_{\mathrm{osc}} t_2), \ldots, A\sin(2\pi f_{\mathrm{osc}} t_N). \tag{28}$$

First, we will analyze the effect of ε_W for the signature assuming $\varepsilon_S = 0$ and $\varepsilon_J = 0$. The comparison error could happen if the noise is stronger than the oscillation signal. If

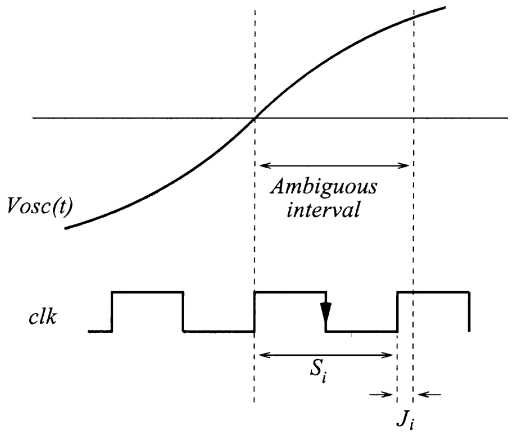


Fig. 10. Ambiguous interval.

TABLE I
AMPLITUDE OF THE FIRST SAMPLE FOR DIFFERENT $f_{\mathrm{osc}} \times T_{\mathrm{TDM}}$ WHEN $A = 1$

$f_{osc} \times T_{TDM}$	$V_{osc}(t_1)$	(dB)
1/10	0.3090	-10.2
1/100	0.0314	-30.1
1/1000	0.00314	-50.1
1/10000	0.000314	-70.1
1/100000	0.0000314	-90.1

$\varepsilon_W(t_i) > V_{\mathrm{osc}}(t_i)$, there could be an error in comparison and inaccurate counting may happen. In general, the comparison error is more likely to happen if $V_{\mathrm{osc}}(t_i)$ is closer to the reference signal. If we assume that $V_{\mathrm{osc}}(t_1)$ is the closest sample to the reference signal, the amplitude of $V_{\mathrm{osc}}(t_1)$ will be $A\sin(2\pi f_{\mathrm{osc}} \times 1/f_{\mathrm{TDM}})$. We can see that the oscillation amplitude will be determined by oscillation frequency f_{osc} times the inverse of TDM clock frequency. Table I shows the amplitude of the first sample for different values of $f_{\mathrm{osc}} \times T_{\mathrm{TDM}}$.

From (15), we can see that $f_{\mathrm{osc}} \times T_{\mathrm{TDM}}$ equals $1/osc\_counter$ if N_{cycles} is one. Therefore, the white noise ε_W will cause an error for the TDM comparator scheme when nominal $osc\_counter$ is significantly large. In order to analyze the effect of noise, the initial samples of (28), which are susceptible to noise, can be rewritten assuming $A = 1$ and $f_{\mathrm{osc}} \times \mathbf{T} = 1/1000$, where $\mathbf{T} = T_{\mathrm{TDM}}$. The approximation is done by $\sin(x) \approx x$ when $x \ll 1$

$$V_{\mathrm{osc}}(t_i) = A\sin(2\pi f_{\mathrm{osc}} 0.5\mathbf{T}), A\sin(2\pi f_{\mathrm{osc}} 1.5\mathbf{T}), \ldots \tag{29}$$

$$\approx A2\pi f_{\mathrm{osc}} 0.5\mathbf{T}, A2\pi f_{\mathrm{osc}} 1.5\mathbf{T}, A2\pi f_{\mathrm{osc}} 2.5\mathbf{T}, \ldots \tag{30}$$

$$\approx 0.003\,14, 0.009\,42, 0.0157, \ldots \tag{31}$$

$$\approx -50.1\ \mathrm{dB}, -40.5\ \mathrm{dB}, -36.1\ \mathrm{dB}, \ldots. \tag{32}$$

The initial samples may be incorrectly counted when the noise power is stronger than the signal power. There will be no incorrect counting after several samples, however, since the signal power is increased as sampling time increases. If we assume that the noise power is -50 dB, which is a pessimistic assumption in most analog circuit designs, only the first sample may be counted incorrectly by our scheme. The incorrect count may reduce the counter value by 1, which causes 0.1% error in the signature when the $osc\_counter = 1000$. As we can see

from the simulations in Section V, it will cause an insignificant error for the fault coverage.

The above analysis was done for only $\varepsilon_W(t)$. Now, if we consider both $\varepsilon_S(t)$ and $\varepsilon_J(t)$ and repeat the equations for $V_{\rm osc}$, then it will be

$$\begin{aligned} V_{\rm osc}(t_i) =& A\sin(2\pi f_{\rm osc}(0.5\mathbf{T}+S_1+J_1)),\\ & A\sin(A\sin(2\pi f_{\rm osc}(1.5\mathbf{T}+S_1+J_2)),\ldots\\ \approx& A2\pi f_{\rm osc}(0.5\mathbf{T}+S_1+J_1),\\ & A\sin(A2\pi f_{\rm osc}(1.5\mathbf{T}+S_1+J_2),\ldots. \end{aligned}$$

For well-designed digital clocks, the amount of jitter will be less than 10% of the clock period. If we assume 10% jitter and the maximum variation of S_1, the possible value of the first two samples can be calculated as

$$0(-\infty\ \text{dB}) \le V_{\rm osc}(t_1) \le 0.006\,91(-43.2\ \text{dB}) \tag{33}$$

$$0.005\,65(-45.0\ \text{dB}) \le V_{\rm osc}(t_2) \le 0.013\,19(-37.6\ \text{dB}). \tag{34}$$

If both S_i and J_i are zero, then the first sampling time will be $0.5T_{\rm TDM}$ from (23), which is the falling edge shown in Fig. 10. However, since we are assuming the maximum variation of ε_S and 10% variation of ε_J, the ambiguous interval for the first sample is from 0 to $1.1 \times T_{\rm TDM}$. It is clear that only the first sample may be affected by -50 dB white noise. The second sample's signal power varies from -45 dB to -37 dB, but it is above the assumed noise power of -50 dB.

Since the clock is not synchronized with $V_{\rm osc}(t)$, the counted value will have the possible error of ± 1. The accuracy of indirect measurement of oscillation frequency can be estimated from (15). By increasing the typical value of $osc\_counter$, the effect of the ambiguous interval can be reduced.

IV. Analysis of Oscillation Behavior

Two important issues are discussed in this section. The first is the differences between the OTM oscillators and the general oscillators. The second is the theoretical analysis of OTM oscillation behavior, which explains why the amplitude measurement is essential.

A. Differences Between OTM Oscillators and General Oscillators

The design of oscillators has been an important topic for communication systems, radio frequency (RF), and phase-locked loop (PLL) circuits [25]–[27]. The OTM oscillator design, however, has significant differences from the general oscillator design. In order to understand the oscillation-test methodology completely, it is essential to analyze the differences. As shown in Fig. 11, the component variations cause the oscillation frequency and amplitude variations. The component variations such as resistance and capacitance variations are represented as $p1$, $p2$, and $p3$. Although the dimensions of component variations could be much higher, they are shown here as three-dimensions for simplicity.

Fig. 11(a) shows a case for a general oscillator design, which has a AGC feedback to control the gain of the nonlinearity. In general, the variations of oscillation frequency and amplitude are minimized by the feedback mechanism in the AGC, while the OTM oscillator in Fig. 11(b) allows the component variations to change its frequency and amplitude. The main goal of a general oscillator designer is to build a circuit that has a well-defined oscillation frequency and amplitude, and to stabilize the frequency and amplitude even if the circuit components vary.

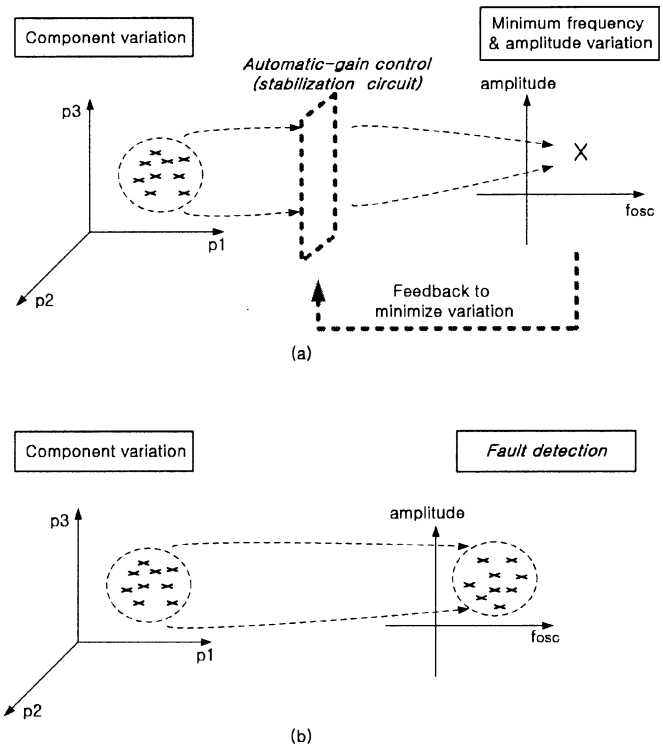


Fig. 11. Variation of oscillators. (a) General oscillators tries to minimize variation. (b) OTM uses the variation to detect faults.

In contrast, the goal of the OTM oscillator designer is significantly different from that of the general oscillator designer. The OTM designer tries to detect the variation of components by measuring the oscillation frequency or amplitude. In other words, the goal is not the stabilization of the oscillator. In addition, any AGC circuit will just hide the information about the component variation and significantly affect the fault detectability. Therefore, it would not make sense to use AGC for OTM. Furthermore, the hardware overhead of an AGC circuit will drastically reduce the advantage of OTM, which is the simplicity of BIST implementation. Simple limiters rather than AGC have been used exclusively in most OTM for these reasons. The limiters are discussed in the next section.

The statistical fault classification techniques [7]–[10] described in Section I can be applied to model the tolerance margin of the oscillation frequency and amplitude in Fig. 11. Applying these techniques can further increase the fault coverage, but the statistical fault classification is beyond the scope of this paper.

B. Describing Function Analysis

The simple linear oscillator design technique is to place poles on the imaginary axis of the complex frequency plane. However, linear oscillators exist only on paper. In practice, parasitics will

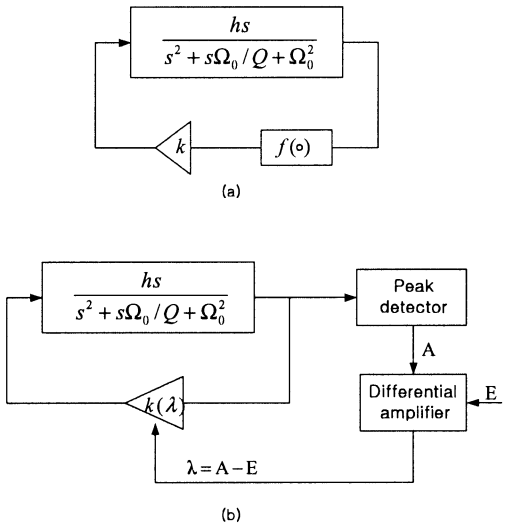


Fig. 12. Bandpass-based oscillator model (a) with a limiting type stabilization scheme and (b) with an AGC scheme.

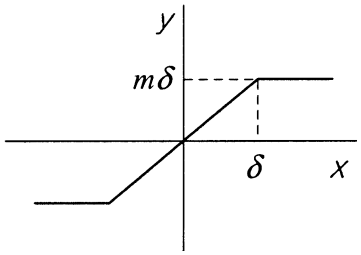


Fig. 13. Saturation function.

TABLE II
ROUTH–HURWITZ LIMIT CYCLE DETERMINATION

Characteristic equation	Limit cycle equations
$s^2 + a_1 s + a_0 = 0$	$a_1 = 0$ $\omega_0^2 = a_0$
$s^3 + a_2 s^2 + a_1 s + a_0 = 0$	$a_1 a_2 - a_0 = 0$ $\omega_0^2 = a_1$
$s^4 + s^3 + a_2 s^2 + a_1 s + a_0 = 0$	$a_1 a_2 a_3 - a_1^2 - a_0 a_3^2 = 0$ $\omega_0^2 = a_1/a_3$

cause the poles to be inside the left half plane. Therefore, any practical oscillator must include some form of regeneration to ensure that the poles are initially located in the right half plane and hence that the oscillation is created [25]–[27], [29]. In addition, the amplitude stabilization mechanism must be added to pull the poles back toward the imaginary axis until a stable value for the amplitude is obtained.

Fig. 12 shows a bandpass-based oscillator model, which consists of a bandpass filter with positive feedback [29]. Oscillation frequency and amplitude control can be implemented with either a limiting type stabilization scheme or an AGC scheme as shown in Fig. 12.

Since all practical oscillators depend on nonlinearities, the well-developed linear system analysis techniques such as the laplace transform cannot be used for oscillator analysis. A common technique for the analysis of nonlinearities is to use the describing function [27]–[29], which relates the input and output of the nonlinear function by linear relationship. By assuming the nonlinearity function $f()$ as an ideal relay and applying the describing function technique, the oscillation frequency ω_0 and amplitude A_0 of the bandpass-based oscillator in Fig. 12 can be expressed as

$$\begin{aligned} \omega_0 &= \Omega_0 \\ A_0 &= \frac{4E_s hQ}{\pi\Omega_0} \end{aligned} \tag{35}$$

where E_s denotes the saturation level of an ideal relay [29].

From these equations, we can clearly see that the oscillation frequency and the oscillation amplitude have different sensitivities to circuit components. The oscillation frequency depends only on the pole frequency Ω_0 of the bandpass filter. The quality factor Q does not affect the oscillation frequency at all, but it determines the oscillation amplitude. This analysis explains why previous research [19], [21], [23] has shown experimental results that the oscillation frequency alone is not sufficient to achieve high fault coverage, and that the measurement of oscillation amplitude is essential to improve the fault coverage. In other words, the oscillation frequency alone can measure only a portion of the circuit specification.

The simplest limiter circuit to implement an oscillator is a digital inverter, which has been commonly used in OTM designs. The opamp's saturation has also been used as a limiter when CUT has high gain [16]. Both techniques are used in the benchmark circuits in Section V. The state variable filter in Fig. 16 [16] has the bandpass gain of 4.5, and saturation is used as a limiter for minimum hardware overhead.

Despite the fact that direct feedback with opamp saturation was used in OTM, no theoretical analysis had been conducted previously. The saturation function in Fig. 13 models the function $f()$ in Fig. 12. The gain k in Fig. 12 is 1 in this case. The describing function for saturation is given in (36) [28]

$$\begin{aligned} N(A) &= mA \le \delta \\ &= \frac{2m}{\pi}\left[\sin^{-1}\left(\frac{\delta}{A}\right) + \left(\frac{\delta}{A}\right)\sqrt{1-\left(\frac{\delta}{A}\right)^2}\right] A > \delta. \end{aligned} \tag{36}$$

When the linear function in the oscillator system is represented as $L(s)$ and the nonlinearity by the describing function $N(A)$, the characteristic equation $1 - N(A)L(s) = 0$ of the positive feedback system will determine the oscillation frequency and amplitude according to the Routh–Hurwitz rule in Table II [28]. The characteristic equation of interest, $1 - N(A)L(s) = 0$ is

$$1 - N(A)\frac{\text{hs}}{\frac{s^2+s\Omega_0}{Q+\Omega_0^2}} = 0 \tag{37}$$

$$1 - \frac{2m}{\pi}\left[\sin^{-1}\left(\frac{\delta}{A}\right) + \left(\frac{\delta}{A}\right)\sqrt{1-\left(\frac{\delta}{A}\right)^2}\right] \times \frac{\text{hs}}{\frac{s^2+s\Omega_0}{Q+\Omega_0^2}} = 0 \tag{38}$$

$$s^2 + \frac{\Omega_0}{Q}s + \Omega_0^2 - \frac{2m}{\pi}\left[\sin^{-1}\left(\frac{\delta}{A}\right) + \left(\frac{\delta}{A}\right)\sqrt{1-\left(\frac{\delta}{A}\right)^2}\right] \text{hs} = 0 \tag{39}$$

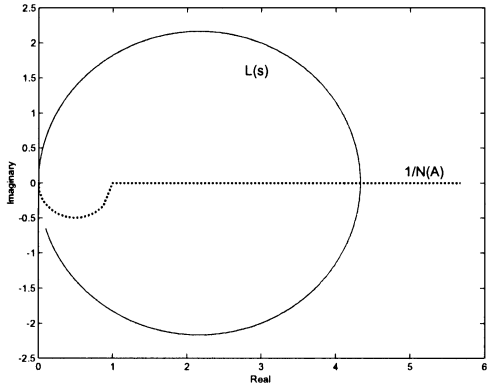


Fig. 14. Polar plot for the state variable filter with $\mathrm{gain} = 4.5$.

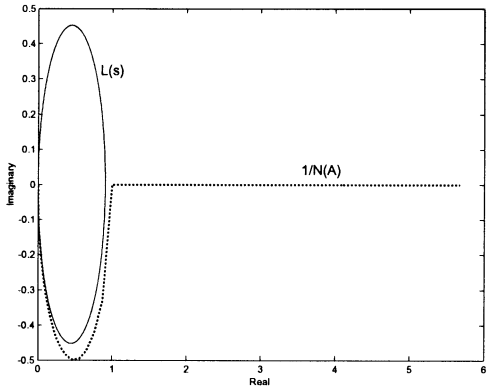


Fig. 15. Polar plot for the state variable filter with $\mathrm{gain} = 0.9$.

where $m = 1$ and $\delta = Vcc/2$, since the saturation of the circuit does not change the gain of the circuit in its operating point, and the saturation level is determined by power supply rails. By using Table II, we can determine the analytical solution of the oscillation frequency ω_0 and amplitude A. When the describing function for the nonlinearity is not simple, polar plots can be useful as a graphical limit cycle determination tool [27], [30]. Figs. 14 and 15 show plots for the bandpass gain of 4.5 and 0.9, respectively, for the same state variable filter architecture. The characteristic equation $1 - N(A)L(s) = 0$ is rearranged, so the circuit's limit cycle can be decided at the point of $L(s) = 1/N(A)$. Fig. 15 does not have any point where two curves intersect, indicating that it will not oscillate.

In general, when the gain is lower than 1, the bandpass circuit is not going to oscillate by the direct feedback connection. In order to convert the CUT into an oscillator in this case, an inverter can be used as a limiter, then the circuit will behave as the bandpass-based oscillator with an ideal relay.

The experimental results in Section V show that the oscillation frequency of the state variable filter is approximately 30% lower than the predicted frequency in the describing function analysis. This discrepancy can be explained by reviewing the limitations in assumptions of the describing function.

1) The describing function analysis has assumed an ideal sinusoidal input to the nonlinear function.
2) The saturation function is ideal and does not have phase lag.
3) The opamp and other circuit components are ideal, in addition to the assumption that no slewing of the opamp happens.

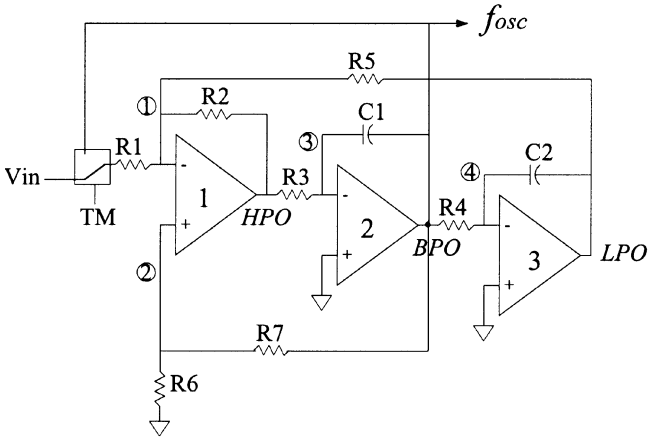


Fig. 16. Testable state variable filter $R_1 = R_2 = R_3 = R_4 = R_5 = 10\,\mathrm{k}\Omega$, $R_6 = 1\,\mathrm{k}\Omega$, $R_7 = 12\,\mathrm{k}\Omega$, $C_1 = C_2 = 20\,\mathrm{nF}$.

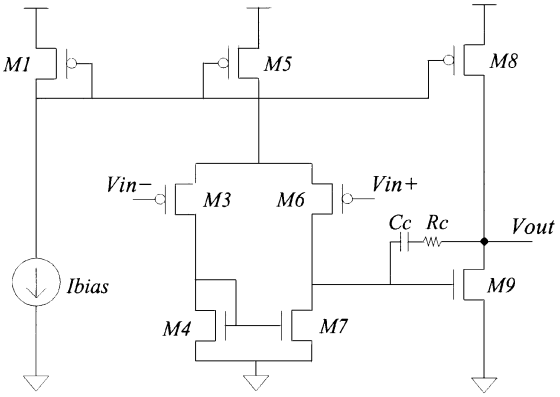


Fig. 17. Two-stage operational amplifier.

The real oscillation frequency and amplitude would deviate from the mathematical analysis since the assumptions for the describing function may not be accurate. For example, the finite slew rate of the real opamp can decrease the oscillation frequency since the phase lag associated with the slew limiting causes a shift in oscillation frequency. Also, the function for the opamp's saturation may have extra phase lag, and the real oscillation frequency is likely to be lower than the frequency that was predicted by the describing function.

The analysis in this section provides a theoretical proof that oscillation amplitude measurement is essential for higher fault coverage. The next section shows the simulation results with the proposed signature analysis technique, which measures both the oscillation frequency and amplitude indirectly.

V. Simulation Results

In this section, simulation results are shown for two benchmark circuits. The state variable filter and the Sallen–Key filter from [16] are used to demonstrate how the fault coverage can be significantly increased by monitoring internal sensitive nodes with less test time.

A. State Variable Filter

Figs. 16 and 17 show a benchmark circuit [16] and its opamp for this simulation, respectively. The state variable filter is converted to an oscillator by controlling test mode (TM) switch.

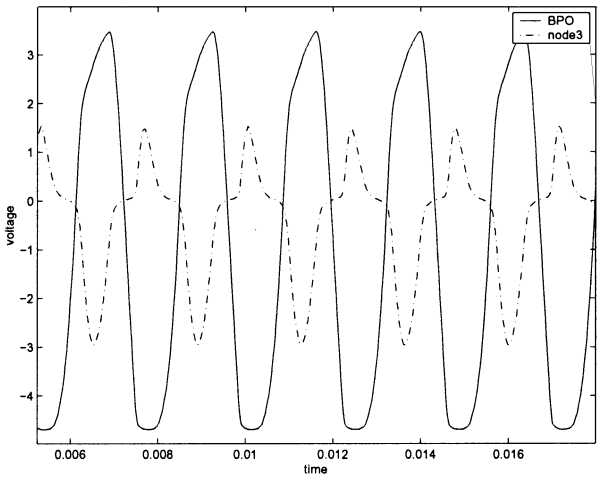


Fig. 18. Oscillation of the CUT in test mode.

TABLE III
TOLERANCE BANDS FOR STATE VARIABLE FILTER

	Osc. Freq. Hz	osc_counter	node 1	Node 2
Nominal	419	2385	216	624
Tolerance	398-438	2281-2514	193-228	556-704

The opamp is a two-stage Miller compensated architecture with a class-A output stage. The oscillation of the CUT in Fig. 18 shows the nominal case oscillation waveforms for the bandpass output (BPO) and the internal node 3. The BPO signal has nominal oscillation frequency of 419 Hz, and its amplitude is clipped by the maximum output swing of the opamp.

It is interesting to notice that node 3 is the virtual ground of the opamp, and it should not have such a large signal transient during normal circuit operation. If we assume that the opamp has infinite output swing, the virtual ground will always perform its ideal small-signal behavior.

However, the practical opamp will have the maximum output swing, and if the oscillation signal approaches the maximum swing, the ideal behavior of opamps will no longer be guaranteed as was discussed in Section III-E. At this point, an ideal integration equation cannot be guaranteed, and the circuit falls into the *virtual ground explosion* state. In Fig. 18, we can see that node 3, which is the virtual ground of opamp 2, starts to explode when the BPO signal starts to clip. The virtual ground explosion happens for other opamp inputs also whenever the output clips.

For these simulations, we use a single-component fault, in which we assume that a single perturbed component causes the output to go beyond its tolerance value. In order to determine the tolerance band, the allowable component deviations are assumed to be $\pm 5\%$ around the nominal value of each component. We calculated the oscillation frequency of the CUT with the variation of each component, and then the variation of oscillation frequency around its nominal frequency is determined as a tolerance band of the CUT. Table III shows tolerance bands for both the traditional OTM and our new analysis test scheme. Comparator outputs with $V_{\rm node1}$ and $V_{\rm node2}$ are inverted to have a small signature value. Tolerance bands for the TDM comparator are determined by the reference voltages in Table IV for the same 5% tolerance for all components.

TABLE IV
REFERENCE VOLTAGES OF THE TDM COMPARATOR FOR STATE VARIABLE FILTER

	voltage level
V_{node1}	-1.0 v
V_{node2}	-1.33 v

TABLE V
MEASUREMENT OF OSCILLATION FREQUENCY USING BOTH DIRECT FREQUENCY MEASUREMENT AND INDIRECT MEASUREMENT FROM $osc\_counter$ VALUE (* DENOTES UNDETECTED FAULTS)

	faulty value	Osc. Freq.	osc_counter	Indirect Frequency
R1	8kΩ	250.13	3997	250.19
	12kΩ	477.78	2092	478.01
R2	8kΩ	* 406.67	* 2458	* 406.83
	12kΩ	* 428.63	* 2333	* 428.63
R3	8kΩ	457.25	2186	457.46
	12kΩ	389.56	2566	389.71
R4	8kΩ	463.39	2157	463.61
	12kΩ	385.36	2594	385.50
R5	8kΩ	491.88	2033	491.88
	12kΩ	330.25	3027	330.36
R6	0.8kΩ	* 400.64	* 2496	* 400.64
	1.2kΩ	* 435.73	* 2294	* 435.92
R7	9.6kΩ	441.11	2266	441.31
	14.4kΩ	* 402.09	* 2486	* 402.25
C1	16nF	466.64	2143	466.64
	24nF	384.47	2600	384.62
C2	16nF	471.70	2119	471.92
	24nF	381.24	2622	381.39

TABLE VI
COMPARISON OF THE MEASUREMENT TIME

	convention scheme	proposed scheme
time	1.0 s	2.4ms

Parametric faults were injected assuming $\pm 20\%$ and $\pm 50\%$ variation of each circuit component. Simulation results in Table V show the signatures for the $\pm 20\%$ parametric faults. The first column shows the components in the circuit, and the second column shows the faulty values. The third column is the direct oscillation frequency measurement from simulations. The fourth column is the $osc\_counter$ value to estimate the frequency indirectly. Equation (15) is used to calculate the indirect frequency in the fourth column.

The frequency of clocks $\phi 1$ and $\phi 2$ in Fig. 5 was 3 MHz and the measurement was done for only one oscillation cycle of the CUT, which takes 2.4 ms. Time-division multiplexing was done with three nodes, the BPO node for the $osc\_counter$ value, and node 1 and node 2 for internal node monitoring. The clock frequency satisfies the minimum requirement in (19).

However, the required test time for the conventional direct measurement of the oscillation frequency needs to be much longer. We assumed a frequency measurement time of 1.0 s since we need sufficient time to detect the small deviation of frequencies. Thus, our approach makes a significant difference in test time, which will result in significant reduction of manufacturing test cost. Table VI shows the comparison of test time.

The clocks for the TDM comparator, $\phi 1$ and $\phi 2$, are each divided into three clocks, $\phi 1$ into $\phi 1a$, $\phi 1b$, and $\phi 1c$, and $\phi 2$ into $\phi 2a$, $\phi 2b$, and $\phi 2c$. The primary output, BPO, and internal nodes, node 1 and 2, were selected as measurement points for the proposed scheme.

TABLE VII
PARAMETRIC FAULT COVERAGE OF STATE VARIABLE FILTER FOR $\pm 20\%$ PARAMETRIC FAULTS (* DENOTES UNDETECTED FAULTS)

	faulty value	Osc. Freq.	osc_ounter	node 1	node 2
R1	8kΩ	250	3997	263	1859
	12kΩ	477	2092	160	461
R2	8kΩ	* 406	2458	**0**	575
	12kΩ	* 428	2333	**265**	656
R3	8kΩ	457	2186	223	599
	12kΩ	389	2566	178	639
R4	8kΩ	463	2157	156	528
	12kΩ	385	2594	246	710
R5	8kΩ	491	2033	274	468
	12kΩ	330	3027	168	967
R6	0.8kΩ	* 400	2496	214	**0**
	1.2kΩ	* 435	2294	218	**724**
R7	9.6kΩ	441	2266	212	725
	14.4kΩ	* 402	2486	217	**0**
C1	16nF	466	2143	198	605
	24nF	384	2600	208	623
C2	16nF	471	2119	161	496
	24nF	381	2622	242	731

TABLE VIII
PARAMETRIC FAULT COVERAGE OF STATE VARIABLE FILTER FOR $\pm 50\%$ PARAMETRIC FAULTS (* DENOTES UNDETECTED FAULTS)

	faulty value	Osc. Freq.	osc_counter	node 1	node 2
R1	5kΩ	0	0	0	0
	15kΩ	532	1878	0	359
R2	5kΩ	378	2639	0	276
	15kΩ	* 438	2281	**325**	682
R3	5kΩ	538	1857	234	526
	15kΩ	356	2804	0	629
R4	5kΩ	573	1744	0	327
	15kΩ	347	2875	285	827
R5	5kΩ	593	1683	423	314
	15kΩ	0	0	0	0
R6	0.5kΩ	366	1331	213	0
	1.5kΩ	458	896	218	759
R7	6.0kΩ	491	765	186	724
	18.0kΩ	382	1232	220	0
C1	10nF	580	753	151	531
	30nF	348	1218	142	582
C2	10nF	640	600	0	143
	30Nf	339	1302	273	869

Simulation results for catastrophic faults show that both direct measurement of oscillation frequency and the proposed indirect scheme have good performance. Both schemes have 100% fault coverage for the catastrophic faults, which include all possible open faults and 30 randomly selected short faults between two nodes. An open fault and a short fault are modeled by a 10 $\mathrm{M}\Omega$ and 1 Ω resistor, respectively.

Even though both schemes have good results for catastrophic faults, we should notice that the test times are significantly different for the two techniques, 2.4 ms and 1.0 s, respectively, in these simulations.

Simulation results in Tables VII and VIII show the signatures for the parametric faults. In this case, since we have oscillation amplitude information for the internal nodes, the fault coverages are significantly higher. Our pass/fail decision was done for the $osc\_counter$ value first. For those undetected faults, the node 1 and node 2 values are compared with the tolerance bands.

The numbers in bold face represent the signatures outside of the tolerance band, which indicate parametric faults detected by the internal node monitoring. The selection of internal nodes is done using the criteria in Section III-D. It is clear that the proposed scheme has higher fault coverage in these simulations. Through internal node monitoring, we detected all $\pm 20\%$ and $\pm 50\%$ parametric faults. The hardware overhead for an extra monitoring circuit is low as explained in Section III.

TABLE IX
DETECTABLE FAULT LIMITS FOR STATE VARIABLE FILTER

	Osc. Freq.	Proposed Scheme
R1	-5% – + 5%	-5% – +5%
R2	-31% – +52%	-5% – +5%
R3	-11% – +14%	-11% – +14%
R4	-9% – +12%	-9% – +8%
R5	-5% – +6%	-5% – +6%
R6	-22% – +24%	-5% – +13%
R7	-18% – +23%	-13% – +5%
C1	-9% – +11%	-9% – +11%
C2	-8% – +10%	-8% – +10%

Table IX shows the detectable fault limits for the state variable filter. The proposed scheme has significantly increased fault coverage by using a TDM comparator for the primary output and internal node monitoring. The internal monitoring nodes were specifically determined to detect the faults in R2, R6, and R7 in Table V. If even higher fault coverage is desired, additional monitoring could be done to further increase the fault coverage.

Fig. 19 shows the sensitivity of the oscillation frequency and the amplitude for the primary output and two internal nodes. The $osc\_counter$ was measured at the primary output, which is BPO in these simulations. We can see that the oscillation frequency has significantly different sensitivity for each component. For example, the R2 variation shows that the sensitivity of the oscillation frequency is low to the faults in R2. However, the sensitivity of node 1 is significantly higher. For the undetected faults in Table V, monitoring of node 1 and node 2 helps to increase the fault coverage significantly.

It should be noted again that the hardware overhead of the proposed scheme for internal node monitoring of oscillation frequency and amplitude would only be the two extra switches for the TDM comparator in the analog block. An extra counter would be the hardware overhead in the digital block.

B. Sallen–Key Filter

The Sallen-Key low-pass filter in Fig. 20 was used as the second benchmark circuit for the simulation. The reference voltages and tolerance bands are shown in Tables X and XI, respectively. In test mode, the negative feedback was applied through the inverter [16]. Simulation results in Table XII shows the signatures for the $\pm 20\%$ parametric faults. The accuracy of the indirect frequency measurement is again very high for the Sallen–Key filter.

The tolerance bands were determined by the same 5% tolerance for all components, as was done for the state variable filter. The same techniques were applied to increase the parametric fault coverage. During the testability analysis stage, five undetected faults were identified as seen in Table XIII. These parametric faults can be detected by monitoring node 2 and node 4. The selection of the internal nodes was done as in the previous section. Table XIV shows the measurement time for the Sallen–Key filter. The measurement of the proposed scheme was done for one oscillation cycle, but it can be repeated for several cycles to increase the tolerance to noise as was mentioned previously.

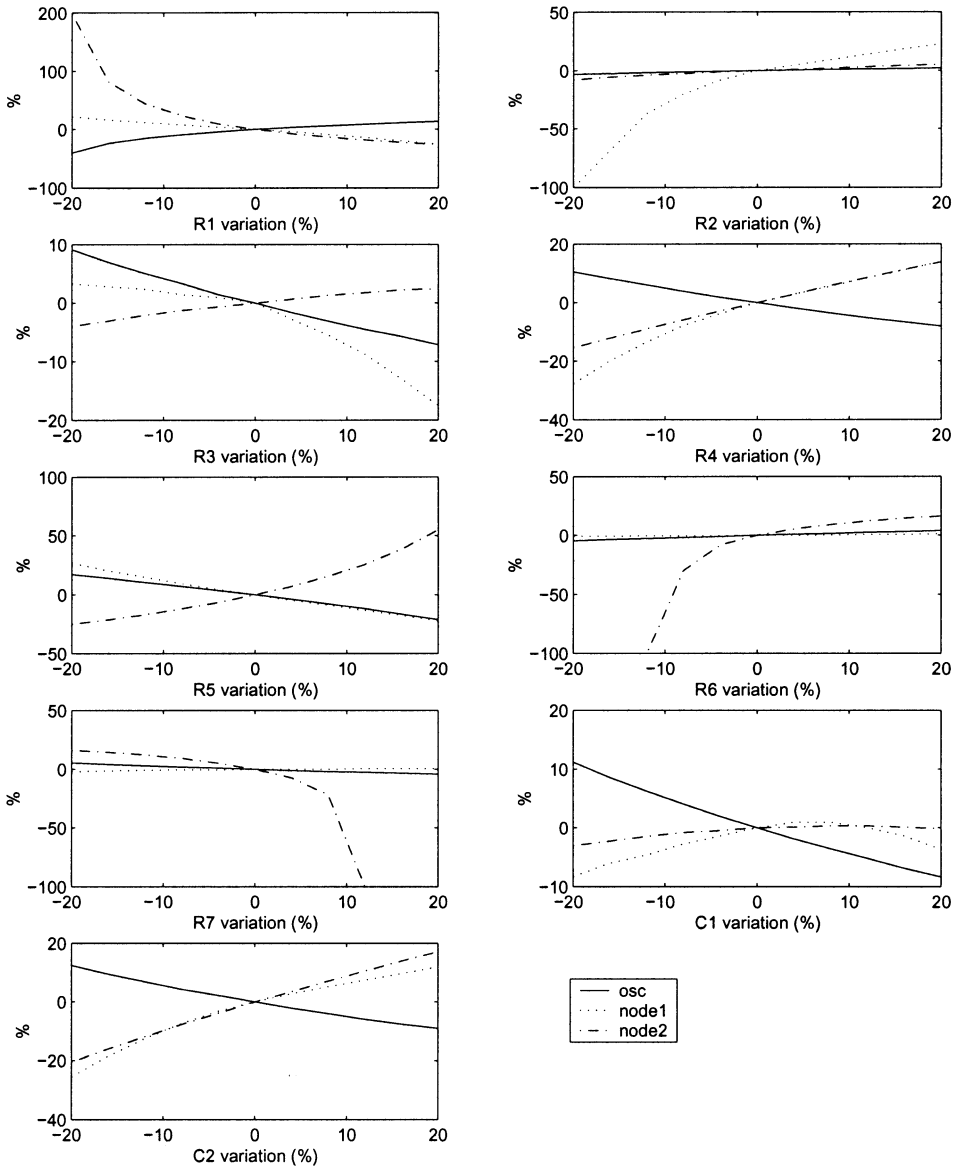


Fig. 19. Signature sensitivities of the state variable filter.

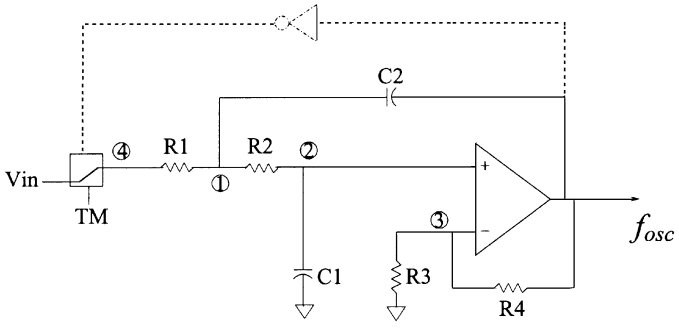


Fig. 20. Testable Sallen-Key filter. TM: Test-mode signal, $R_1 = R_2 = 3.2\ \mathrm{k}\Omega$, $R_3 = 4.86\ \mathrm{k}\Omega$, $R_4 = 8.84\ \mathrm{k}\Omega$, $C_1 = C_2 = 50\ \mathrm{nF}$.

TABLE X
REFERENCE VOLTAGES OF THE TDM COMPARATOR FOR SALLEN–KEY FILTER

	voltage level
V_{node2}	-0.1 v
V_{node4}	0.6 v

TABLE XI
TOLERANCE BANDS FOR SALLEN–KEY FILTER

	Osc. Freq. Hz	osc_counter	node 2	Node 4
Nominal	1028	973	242	112
Tolerance	962-1101	908-1039	229-253	54-162

For the $\pm 20\%$ parametric faults, direct frequency measurement results in five undetected faults. By monitoring extra nodes, it is possible to detect all undetected parametric faults. Fig. 21 shows the sensitivity of the oscillation frequency and the internal nodes for the Sallen–Key filter. Since the faults in R1, R2, and C1 are undetected in Table XIII, the adjacent nodes, node 2 and node 4, are monitored.

With a direct frequency measurement technique, the OTM has three undetected faults even for $\pm 50\%$ parametric faults

TABLE XII
MEASUREMENT OF OSCILLATION FREQUENCY USING BOTH DIRECT FREQUENCY MEASUREMENT AND INDIRECT MEASUREMENT FROM *osc_counter* VALUE (* DENOTES UNDETECTED FAULTS)

	faulty value	Osc. Freq.	osc_counter	Indirect Frequency
R1	8kΩ	* 1038.4	* 963	* 1038.4
	12kΩ	* 1015.2	* 985	* 1015.2
R2	8kΩ	* 1067.2	* 937	* 1067.2
	12kΩ	* 988.1	* 1012	* 988.1
R3	8kΩ	871.0	1148	871.1
	12kΩ	1204.8	830	1204.8
R4	8kΩ	1335.1	749	1335.1
	12kΩ	878.7	1137	879.5
C1	16nF	* 972.7	* 1028	* 972.8
	24nF	1116.0	896	1116.1
C2	16nF	1396.6	716	1396.6
	24nF	818.3	1222	818.3

TABLE XIII
PARAMETRIC FAULT COVERAGE OF SALLEN–KEY FILTER FOR $\pm 20\%$ PARAMETRIC FAULTS (* DENOTES UNDETECTED FAULTS)

	faulty value	Osc. Freq.	osc_counter	node 2	node 4
R1	2.56kΩ	* 1038	963	235	**45**
	3.84kΩ	* 1015	985	249	**163**
R2	2.56kΩ	* 1067	937	**224**	122
	3.84kΩ	* 988	1012	**258**	106
R3	3.89kΩ	871	1148	253	268
	5.83kΩ	1204	830	233	0
R4	7.07kΩ	1335	749	222	0
	10.61kΩ	878	1137	254	263
C1	40nF	* 972	1028	240	**196**
	60nF	1116	896	237	0
C2	40nF	1396	716	189	0
	60nF	818	1222	288	220

TABLE XIV
COMPARISON OF THE MEASUREMENT TIME

	convention scheme	proposed scheme
time	1.0s	0.97ms

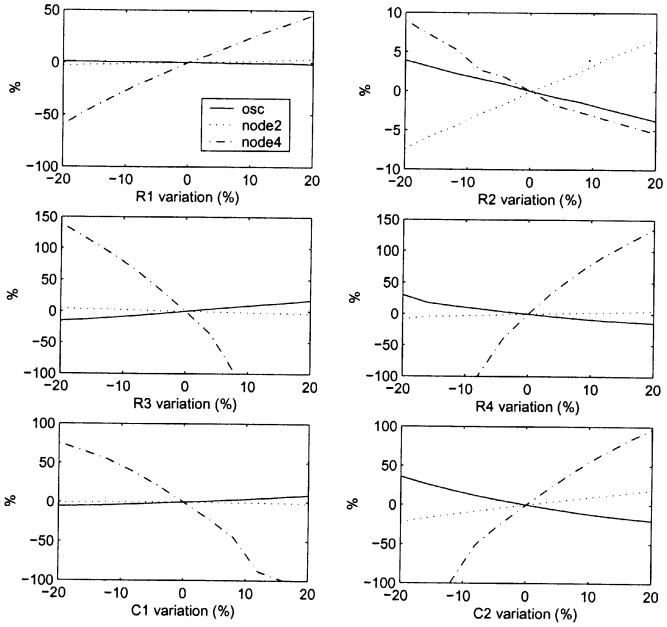


Fig. 21. Signature sensitivities of the Sallen–Key filter.

as can be seen in Table XV. This emphasizes again the importance of an efficient signature analysis scheme to improve the test quality.

TABLE XV
PARAMETRIC FAULT COVERAGE OF SALLEN–KEY FILTER FOR $\pm 50\%$ PARAMETRIC FAULTS (* DENOTES UNDETECTED FAULTS)

	faulty value	Osc. Freq.	osc_counter	node 2	node 4
R1	1.6kΩ	* 1046	956	227	**0**
	4.8kΩ	* 990	1010	262	**222**
R2	1.6kΩ	1152	868	195	128
	4.8kΩ	936	1068	280	103
R3	2.43kΩ	726	1377	274	451
	7.29kΩ	1709	584	163	0
R4	4.42kΩ	0	0	0	0
	13.26kΩ	775	1288	268	395
C1	25nF	* 982	1017	222	**242**
	75nF	1529	653	88	0
C2	25nF	0	0	0	0
	75nF	649	1540	348	328

TABLE XVI
DETECTABLE FAULT LIMITS FOR SALLEN–KEY FILTER

	Osc. Freq.	Proposed Scheme
R1	short – +61%	-17% – +20%
R2	-35% – +32%	-15% – +9%
R3	-6% – +8%	-6% – +8%
R4	-7% – +7%	-7% – +7%
C1	-70% – +18%	-10% – +9%
C2	-6% – +5%	-6% – +5%

Table XVI reveals that the OTM would have significant limitations in the fault coverage for several components. Especially for the faults in R1, even the short fault did not cause the oscillation frequency to deviate significantly. As we can see in Fig. 21, node 4 has higher sensitivity to variations in R1.

VI. CONCLUSION

A comprehensive signature analysis scheme with minimum hardware overhead is proposed for oscillation-test methodology. With the TDM technique, we can select internal test nodes with only a simple switch and a counter for each test node. By monitoring sensitive internal nodes, we can have sufficient information to detect all catastrophic faults and most of the parametric faults. It is shown that the TDM comparator scheme significantly reduces the test time of oscillation-test with higher fault coverage. As an efficient BIST technique, the TDM comparator scheme measures the oscillation frequency as well as the amplitude of oscillation. In general, the maximum output signal swing of the operational amplifier will limit the oscillation amplitude, which makes the amplitude measurement a difficult problem. We have showed that this problem can be solved by measuring the internal node during the *virtual ground explosion* state, which we have explained using the benchmark circuit. We have also provided the describing function analysis to show that the amplitude measurement is essential for high fault coverage. With the state variable filter and Sallen-Key filter in our simulations, fault coverage for all open faults and randomly selected short faults is 100%. We also showed that the fault coverage for $\pm 20\%$ and $\pm 50\%$ parametric faults can be increased up to 100% by monitoring internal sensitive nodes.

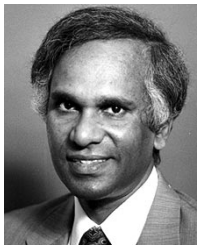
REFERENCES

[1] M. F. Toner and G. W. Roberts, "A BIST scheme for an SNR test of a sigma-delta ADC," in *Proc. IEEE Int. Test Conf.*, 1993, pp. 805–814.
[2] B. Dufort and G. W. Roberts, "Signal generation using periodic single and multi bit sigma-delta modulated streams," in *Proc. IEEE Int. Test Conf.*, 1997, pp. 396–405.

[3] C. Y. Pan and K. T. Cheng, "Pseudorandom testing for mixed-signal circuits," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 1173–1185, Oct. 1997.
[4] P. N. Variyam, A. Chatterjee, and N. Nagi, "Low-cost and efficient digital-compatible BIST for analog circuits using pulse response sampling," in *Proc. IEEE VLSI Test Symposium*, 1997, pp. 261–266.
[5] N. Nagi, A. Chatterjee, H. Yoon, and J. A. Abraham, "Signature analysis for analog and mixed-signal circuit test response compaction," *IEEE Trans. Computer-Aided Design*, vol. 17, pp. 540–546, June 1998.
[6] J. Roh and J. A. Abraham, "Subband filtering scheme for analog and mixed-signal circuit testing," in *Proc. IEEE Int. Test Conf.*, 1999, pp. 221–229.
[7] W. M. Lindermeir, H. E. Graeb, and K. J. Antreich, "Analog testing by characteristic observation inference," *IEEE Trans. Computer-Aided Design*, vol. 18, pp. 1353–1368, Sept. 1999.
[8] B. R. Epstein, M. Czigler, and S. R. Miller, "Fault detection and classification in linear integrated circuits: An application of discrimination analysis and hypothesis testing," *IEEE Trans. Computer-Aided Design*, vol. 12, pp. 102–113, Jan. 1993.
[9] Z. Wang, G. Gielen, and W. Sansen, "Probabilistic fault detection and the selection of measurements for analog integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. 17, pp. 862–872, Sept. 1998.
[10] Z. R. Yang, M. Zwolinski, C. D. Chalk, and A. C. Williams, "Applying a robust heteroscedastic probabilistic neural network to analog fault detection and classification," *IEEE Trans. Computer-Aided Design*, vol. 19, pp. 142–151, Jan. 2000.
[11] K. Arabi and B. Kaminska, "Testing analog and mixed-signal integrated circuits using oscillation-test method," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 745–753, July 1997.
[12] ——, "Parametric and catastrophic fault coverage of analog circuits in oscillation-test methodology," in *Proc. IEEE VLSI Test Symp.*, 1997, pp. 166–171.
[13] ——, "Oscillation built-in self test (OBIST) scheme for functional and structural testing of analog and mixed-signal integrated circuits," in *Proc. IEEE International Test Conf.*, 1997, pp. 786–795.
[14] ——, "Built-in temperature sensors for on-line thermal monitoring of microelectronics structures," in *Proc. IEEE Int. Conf. Computer Design*, 1997, pp. 462–467.
[15] ——, "Design for testability of embedded integrated operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 33, pp. 573–581, Apr. 1998.
[16] ——, "Oscillation-test methodology for low-cost testing of active analog filters," *IEEE Trans. Instrumen. Meas.*, vol. 48, pp. 798–806, Aug. 1999.
[17] I. H. S. Hassan, K. Arabi, and B. Kaminska, "Testing digital to analog converters based on oscillation-test strategy using sigma-delta modulation," in *Proc. IEEE Int. Conf. Computer Design*, 1998, pp. 40–46.
[18] D. Vazquez, A. Rueda, J. L. Huertas, and E. Peralias, "A high-Q bandpass fully differential SC filter with enhanced testability," *IEEE J. Solid-State Circuits*, vol. 33, pp. 976–986, July 1998.
[19] G. Huertas, D. Vazquez, A. Rueda, and J. L. Huertas, "Effective oscillation-based test for application to a DTMF filter bank," in *Proc. IEEE Int. Test Conf.*, 1999, pp. 549–555.
[20] M. S. Zarnik, F. Novak, and S. Macek, "Design of oscillation-based test structures for active RC filters," in *IEE Proc.–Circuits Devices Syst.*, vol. 147, 2000, pp. 297–302.
[21] M. W.-T. Wong, "On the issues of oscillation test methodology," *IEEE Trans. Instrum. Meas.*, vol. 49, pp. 240–245, Apr. 2000.
[22] J. Roh and J. A. Abraham, "A comprehensive TDM comparator scheme for effective analysis of oscillation-based test," in *Proc. IEEE VLSI Test Symp.*, Apr. 2000, pp. 143–148.
[23] D. Vazquez, G. Huertas, G. Leger, A. Rueda, and J. L. Huertas, "Practical solutions for the application of the oscillation-based test: Start-up and on-chip evaluation," in *Proc. IEEE VLSI Test Symp.*, Apr. 2002, pp. 143–148.
[24] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.
[25] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, MA: Addison-Wesley, 1978.
[26] L. O. Chua, C. A. Desoer, and E. S. Kuh, *Linear and Nonlinear Circuits*. New York: McGraw-Hill, 1987.
[27] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[28] A. Gelb and W. Vander Velde, *Multiple-Input Describing Functions and Nonlinear System Design*. New York: McGraw-Hill, 1968.
[29] A. Rodriguez-Vazquez, B. Linares-Barranco, J. L. Huertas, and E. Sanchez-Sinencio, "On the design of voltage-controlled sinusoidal oscillators using OTA's," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 198–211, Feb. 1990.
[30] J-J. E. Slotine and W. Li, *Applied Nonlinear Control*. Englewood Cliffs, NJ: Prentice-Hall, 1991.
[31] *Matlab Version 6.0*, The MathWorks, Inc., 2000.
[32] A. G. F. Dingwall, "Monolithic expandable 6 bit 20 MHz CMOS/SOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 926–932, Dec. 1979.
[33] B. Song and P. R. Gray, "A precision CMOS bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 634–643, Dec. 1983.
[34] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. Oxford, U.K.: Oxford Univ. Press, 2002.

Jeongjin Roh received the B.S. degree in electrical engineering from the Hanyang University, Seoul, Korea, in 1990, the M.S. degree in electrical engineering from the Pennsylvania State University, in 1998, and the Ph.D. degree in computer engineering from the University of Texas, Austin, in 2001.

From 1990 to 1996, he was with Samsung Electronics, Kiheung, Korea, where he was a Senior Circuit Designer for several mixed-signal products. From 2000 to 2001, he was a Senior Analog Designer with the Intel Corporation, Austin, TX, where he worked on wireless communication circuits. In 2001, he joined the faculty at the Hanyang University, Ansan, Korea. His research interests include low-power analog circuits, oversampled delta-sigma converters, and modeling and testing of analog and mixed-signal circuits.



Jacob A. Abraham (S'71–M'74–SM'84–F'85) received the B.S. degree in electrical engineering from the University of Kerala, Kerala, India, in 1970 and the M.S. degree in electrical engineering and Ph.D. degree in electrical engineering and computer science from Stanford University, Stanford, California, in 1971 and 1974, respectively.

He is a Professor in the Departments of Computer Sciences and Electrical and Computer Engineering, University of Texas, Austin. He is also the Director of the Computer Engineering Research Center and holds a Cockrell Family Regents Chair in Engineering. From 1975 to 1988, he was on the faculty of the University of Illinois, Urbana. He has over 300 publications and has supervised more than 50 Ph.D. dissertations. His research interests include VLSI design and test, formal verification, and fault-tolerant computing. He is the principal investigator of several contracts and grants in these areas, and a consultant to industry and government on testing and fault-tolerant computing.

Professor Abraham has been elected Fellow of the ACM. He served as Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON VLSI SYSTEMS, and was chair of the IEEE Computer Society Technical Committee on Fault-Tolerant Computing in 1992 and 1993.