A Continuous-Time Delta-Sigma Modulator
for High Speed Signal Processing

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Continuous-time delta-sigma modulator has been designed using excess loop compensation technique. The designed modulator shows 70.0 dB SNDR within 20 MHz signal bandwidth. The delta-sigma modulator has been implemented 65 nm process. Designed amplifier for implementing the high speed delta-sigma modulator has 45-dB DC gain and 2-GHz unity-gain frequency. The implemented circuit of the continuous-time delta-sigma modulator has been designed by using MATLAB, Cadence, Spectre, HSPICE, and PADS PCB tools.

Fig 1. (a) 3rd order 4-bit continuous time delta sigma ADC architecture  (b) DAC shape (NRZ, RZ)
The modulator structure used in this paper is shown in Fig 1 (a). In case of continuous-time delta sigma structure, it is sensitive to clock jitter and excess loop delay. To compensate for these drawbacks, the first DAC uses the non-return to zero (NRZ) scheme to reduce the effects of clock jitter, while the second DAC and third DAC generate RZ (Return to Zero) pulses to compensate for excess loop delay. In addition, local feedback was used to reduce the effects of noise by moving zero around the signal band [1]-[2].

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