A 0.9-V 60-μW 1-Bit Fourth-Order Delta-Sigma Modulator With 83-dB Dynamic Range

Jeongjin Roh, Member, IEEE, Sanho Byun, Younkil Choi, Student Member, IEEE, Hyungdong Roh, Student Member, IEEE, Yi-Gyeong Kim, and Jong-Kee Kwon, Member, IEEE

Abstract—A 0.9-V 60-μW delta-sigma modulator is designed using standard CMOS 0.13-μm technology. The modulator achieves 83-dB dynamic range in a signal bandwidth of 20 kHz with a sampling frequency of 2 MHz. The input-feedback architecture is used to reduce the voltage swing of the integrators, which enables low-power amplifiers. By considering the characteristics of the modulator architecture, low-quinsect operational transconductance amplifiers are designed, which use positive feedback to increase dc gain. The designed modulator shows very high figure of merit among the state-of-the-art sub-1-V modulators.

Index Terms—Low power, low voltage, operational transconductance amplifier, sigma-delta modulation, switched capacitor circuits.

I. INTRODUCTION

The design of low-voltage low-power delta-sigma data converters has been an important academic and industrial issue for more than a decade [1]. Recently, the proliferation of battery-operated systems has demanded even more power-efficient circuits than ever. Sub-1-V delta-sigma modulators have been presented in many papers [2]–[6], and our work shows a 0.9-V design with only 60-μW for the 83-dB dynamic range. A common technique for low-voltage design is to use charge pumps to generate higher voltage than the supply voltage for switches [7], [13]. Another popular technique is the switched-op amp instead of charge pumps [2], [3].

However, a recent process development has enabled low-threshold voltage transistors for modulator design [8], [9], which eliminate the need for charge pumps or switched-op amps. We used low-threshold voltage devices of a 0.13-μm CMOS process, and this enables a simple circuit design, which in turn enables a more power-efficient modulator. We also exploit the advantage of the feedforward modulator for low-power circuit design. Feedforward modulator architecture has gained popularity recently because of the small voltage swings in the loop filter of the modulator. This allows extra room for more efficient circuit design. By combining the advantages of feedforward architecture and the loop-power operational transconductance amplifier (OTA), the implemented modulator achieves very high figure-of-merit (FOM) among the state-of-the-art modulators.

Section II discusses the details of the architectural issues for low-power design. The effect of the parasitic integrator caused by the parasitic capacitance at the input node of the comparator is analyzed, the leakage current issue is addressed, and the requirements of the OTA specifications are discussed. Section III then shows the circuit blocks used in the modulator. Details of the circuit design are provided in this section. Section IV has measurement results and is followed by the conclusion.

II. ARCHITECTURAL DESIGN

In this section, architectural and circuit design issues will be discussed for low-power circuit design. First, the design of modulator topology is explained. The effect of the feedforward topology for low-power design is analyzed. The architectural issue and leakage current are discussed. The design requirement of an OTA is also presented that considers the property of the feedforward topology.

A. Modulator Topology

Most of the low-voltage modulators have been implemented using feedback architectures. Instead of the feedback architecture, our design employs the input-feedback architecture, which has become popular in recent years [10]–[12]. The feedforward architecture has an extra signal path from the input of the modulator to the quantizer. This simple architectural modification can have significant impact on analog circuit design.

The signal component, which appears in the loop filter of the conventional modulator, is completely removed in the feedforward modulator. This feature makes the feedforward architecture very attractive. The analog circuits do not need to have large voltage swings, so the design requirement of the OTA becomes relaxed. We have used this feature to design a very low-power modulator, as explained in Sections II-B–E and III.

There should be several important choices in designing a delta-sigma modulator architecture. The order of a modulator, the oversampling ratio, the choice between a single-loop or cascaded modulator, and the choice between a single-bit or multibit quantizer are all important decisions to make [13], [14]. Our design goal is to design a highly power-efficient modulator, and it is realized that complex modulator architecture would require high power to make it function properly. For example, cascaded modulators require more stringent analog components such as high-performance OTAs. Multibit architecture requires the dynamic element matching (DEM) technique, which also requires extra current consumption for the extra...
The NTF of the designed modulator can be calculated as

\[
\text{NTF}(z) = \frac{A(z)}{B(z)} = \frac{A_4 z^4 + A_3 z^3 + A_2 z^2 + A_1 z + A_0}{B_4 z^4 + B_3 z^3 + B_2 z^2 + B_1 z + B_0}
\]

(1)

where

\[
\begin{align*}
A_4 &= 1 \\
A_3 &= -4 \\
A_2 &= 6 + a_4 g \\
A_1 &= -4 - 2a_4 g \\
A_0 &= 1 + a_4 g \\
B_4 &= 1 \\
B_3 &= -4 + a_1 b_1 \\
B_2 &= 6 + a_4 g - 3a_1 b_1 + a_1 a_2 b_2 \\
B_1 &= -4 - 2a_4 g + 3a_1 b_1 - 2a_1 a_2 b_2 + a_1 a_4 b_1 + a_1 a_2 a_3 b_3 \\
B_0 &= (1 + a_4 g)(1 - a_1 b_1 + a_1 a_2 b_2) + a_1 a_2 a_3(a_4 b_1 - b_3).
\end{align*}
\]

The local feedback loop with a gain coefficient of \( g \), which forms a resonator, is to move a pair of the NTF zeros to the edge of the signal band. The coefficients of the designed modulator are summarized in Table I. The ideal output spectrum of a behavioral simulation is shown in Fig. 2 with these coefficients. It clearly shows a notch in the spectrum caused by the resonator.

**B. Effect of the Parasitic Capacitance of the Comparator**

The feedforwarded integrator outputs are summed at the comparator input node with proper switch clocking. The parasitic capacitor at the input node of the comparator stores the summation output during the comparator’s evaluation time. Then the stored charge is summed with the feedforwarded voltages at the next clock to determine the comparator output. The capacitor at the input node of the comparator combined with the switch forms the parasitic fifth integrator as shown in Fig. 3. The integrator coefficient \( a_5 \) is determined by the ratio of the parasitic capacitance to the total capacitance at the comparator input node. This parasitic integrator has the benefit of...
increasing the noise shaping property by increasing the order of the modulator from four to five.

\[
\text{NTF}_{\text{new}}(z) = \frac{B'(z)(z - a_5)}{B(z)z - A(z)a_5}
\]  

(2)

The analysis of the modulator in Fig. 3 shows that the new NTF in (2) is different from (1), where \(a_5\) is determined by the size of parasitic capacitor. The locations of the original four zeros are fixed while the locations of the extra fifth zero is determined by the parasitic capacitance. Fig. 4 shows that the movement of fifth zero. If there is no parasitic capacitor, the NTF is as that of the fourth-order modulator, as expected. However, the fifth zero moves to the right on the real axis as the parasitic capacitance increases. This extra zero has the benefit of increased noise-shaping action as shown in Fig. 5. The attenuation of the quantization noise in the signal band is slightly increased.

A concern about the parasitic capacitor is the stability of the modulator. The modulator becomes a fifth-order system by the parasitic integrator, and the stability problem can arise. The NTF peak value increases from 1.5 to 1.8 as the parasitic capacitance changes from 0 to 200 fF. If the NTF peak increases too much, the feedback system can become unstable [14]. In our design, the estimated total capacitance is less than 100 fF, which does not affect the stability.

C. Integrator Output Swings

Since the presented modulator is optimized to use the feature of low-voltage swing at the input of the loop filter, it is essential to watch the voltage swings at the outputs of the integrators. A behavioral simulation with a half-scale input signal is performed to show the integrator output swings as in Figs. 6 and 7. The figures show scaled output swings to the full-scale reference.
Devices are causing leakage problems above 45 dB, the modulator’s SNR does not degrade. The SNR variation does not affect the SNR significantly. If the gain is increased to the –120 dB level. The op amp’s finite dc gain moves the NTF zero from dc to a higher frequency [14], and the effects of thermal noise and clock jittering are combined to increase the noise floor. As expected, the nonlinear leakage current causes harmonic distortion in our simulation. Fig. 12 shows the simulation result with and without the leakage current. The simulation result with the leakage current clearly shows harmonic distortions.

As the leakage current becomes a problem, complex switching techniques have been proposed to prevent the leakages [19]. However, the proposed techniques use complex switches instead of simple CMOS or nMOS switches. Sometimes even the negative voltage is generated to turn off the switch completely. After careful consideration of those switches, we have decided to use simple conventional switches for circuit simplicity and power efficiency at the cost of additional harmonic distortions.

III. CIRCUIT IMPLEMENTATION

The key analog building blocks in the modulator are explained in this section. The OTA is the most critical block, and is explained first. Other important blocks are subsequently explained.

A. Low-Power High-Performance OTA

The most critical part of the delta-sigma modulator is the operational transconductance amplifiers (OTAs). In particular, the first OTA has dominant impact on modulator performance, hence, the first OTA consumes about half or sometimes more than half of the total power.

The behavioral simulations with nonidealities showed that the noise floor is increased to the –120 dB level. The op amp’s finite dc gain moves the NTF zero from dc to a higher frequency [14], and the effects of thermal noise and clock jittering are combined to increase the noise floor. As expected, the nonlinear leakage current causes harmonic distortion in our simulation. Fig. 12 shows the simulation result with and without the leakage current. The simulation result with the leakage current clearly shows harmonic distortions.

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The class-AB circuit is known to be more power efficient; therefore, it is a widely used OTA architecture [2], [9]. However, a drawback of the class-AB architecture is that it requires extra circuit to provide battery voltage to control the quiescent current of the pMOS and nMOS output transistors. For accurate control of low-quiescent current consumption, a process-voltage-temperature (PVT) independent battery circuit is required, which unavoidably increases total quiescent current. To reduce extra quiescent current increase, sometimes the gate-source voltage of the source follower is used as a battery voltage [9]. This has the advantage of simple circuit design; however, it has PVT dependency, and modulator performance could vary inevitably. Our
Fig. 9. Behavioral model in Simulink.

Fig. 10. HSPICE simulation result of switch leakage current.

Fig. 11. Leakage current model in Simulink.

design goal is to minimize power consumption; therefore, complex circuitry to implement a class-AB OTA is avoided.

Another important design criteria in an OTA is the high-gain and wide bandwidth not only for the integrator settling but also for the high power supply rejection ratio (PSRR). The folded-cascode amplifier is one of the most popular selections in delta-sigma modulators [11]. It achieves high-gain by transistor cascoding without multistage amplification. Because of its single-stage nature, the frequency compensation is achieved by a load capacitor in a switched-capacitor circuit. However,
Fig. 13. Schematic of the first OTA. (NMOS unit size $W/L = 0.4/0.8$, and pMOS unit size $W/L = 2.2/2.0$ unless otherwise noted. Units are in $\mu$m).

**TABLE II**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>OTA1</th>
<th>Other OTAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V)</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>Static supply current ($\mu$A)</td>
<td>22.7</td>
<td>53</td>
</tr>
<tr>
<td>DC gain (dB)</td>
<td>55</td>
<td>43</td>
</tr>
<tr>
<td>Phase margin (degree)</td>
<td>29</td>
<td>66</td>
</tr>
<tr>
<td>Load capacitor ($C_{\text{pff}}$) (pF)</td>
<td>3</td>
<td>0.8</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>37</td>
<td>14</td>
</tr>
</tbody>
</table>

Fig. 14. First integrator’s settling behavior.

transistor cascoding requires extra voltage headroom, and is usually avoided in low-voltage design.

In our circuit design, which is shown in Fig. 13, we use a simple single-stage class-A architecture with local positive feedback [15], [16] to increase amplifier gain and gain-bandwidth product (GBW) as

$$A_I = g_{m1}R_{\text{out}} \times \frac{B}{1 - \alpha}$$  \hspace{0.5cm} (3)

$$\text{GBW} = \frac{g_{m1}B}{2\pi C_L(1 - \alpha)},$$  \hspace{0.5cm} (4)

where $\alpha = (W/L)_3/(W/L)_2$, $B = (W/L)_4/(W/L)_2$, and $R_{\text{out}}$ is the output resistance of the OTA. In the above equations, we ignore the effect of the drain-source resistances of the input pair and the current steering transistors since the resistances are large because of the small amount of current and relatively large transistor lengths. If the amount of positive feedback is larger than 1, the circuit becomes a latch. In this design, the parameters are $\alpha = 0.8$ and $B = 6$ for the first OTA. A reasonable value for $\alpha$ is 0.75, and a practical maximum value for $\alpha$ is 0.9, because beyond that any mismatches may cause the value of $\alpha$ to
Fig. 18. Schematic of the presented fourth-order modulator.

Table II shows the simulation results of the designed OTAs. In order to evaluate the performance of the OTAs in the capacitive feedback configuration, the effective load capacitances, $C_{L,eff}$, are estimated. In our circuit configuration, the OTAs in the sampling phase, when $\Phi_1$ is high, have lower $C_{L,eff}$, which means that they will have a lower phase margin than in the integrating phase. The equation for $C_{L,eff}$ is shown below [14], [17]

$$C_{L,eff} = C_L + \frac{C_I \times C_P}{C_I + C_P}$$

where $C_L$ is the load capacitance, $C_I$ is the integrating capacitance, and $C_P$ is the parasitic capacitance at the OTA input node. With the estimated effective load capacitance of 3 pF, the first OTA has 55-dB DC gain and 37-MHz GBW, which is sufficient for our modulator, as shown in Fig. 8. With the 3-pF load capacitor, the phase margin of the first OTA is the relatively low value of 29°. During the $\Phi_1$ cycle, the first OTA drives the sampling capacitor of the second integrator, which is only 0.4 pF. Since the phase margin is low, the OTA input and output voltage have slight ringing at the beginning of the clock cycle as shown in Fig. 14. However, even though there is some ringing, we have confirmed from circuit simulation that the circuit settles with sufficient accuracy. Instead of reducing bandwidth to achieve higher phase margin, we designed the circuit to have very high speed operation with a little bit of ringing at the beginning of the clock cycle. The other OTAs are relatively less critical than the first OTA; therefore, the current and performance are scaled down to reduce power consumption.

Fig. 15 shows the switched-capacitor common-mode feedback (SC-CMFB) circuit that is used for the fully-differential circuit implementation [21]. The CMFB circuit senses the output common-mode voltage and provides the control voltage to balance the OTA’s positive and negative outputs. The switches are implemented using nMOS transistors except for the two switches connected to the outputs of the OTA, which are implemented as CMOS switches to accommodate wider voltage swings. The capacitor values in this circuit are 0.1 pF and 0.4 pF for $C_1$ and $C_2$, respectively.

### TABLE III

| Capacitance Values Used in the Modulator (Units are in pF) |
|-----------------|-----------------|-----------------|-----------------|
| Sampling capacitors | Integrating capacitors | Feedforward capacitors | Resonator capacitor |
| $C_{s1}=3$   | $C_{s2}=0.4$   | $C_{s3}=0.96$   | $C_{r1}=0.1$   |
| $C_{s1}=15$  | $C_{s2}=0.8$   | $C_{s3}=2.16$   | $C_{r1}=0.4$   |
| $C_{r3}=0.6$ | $C_{r4}=0.2$   | $C_{r4}=0.15$   | $C_{r4}=0.15$   |

B. Single-Bit Quantizer and SR Latch

The design requirement of a 1-bit comparator can be relaxed in delta-sigma modulators since the nonidealities of the comparator also experience noise-shaping the same as the quantization noise. The comparator in Fig. 16 uses the dynamic latch architecture controlled by a clock signal. When the $\Phi_1$ signal is low, two pMOS transistors pull up the $outp$ and $outn$ nodes,
while the nMOS pull-down path is disconnected. At this timing, both output signals are high, which mandates the use of the SR latch following the comparator. When $\Phi_{14}$ signal goes high, two pMOS pull-up transistors turn off, and at the same time the two nMOS transistors turn on. Now the $\text{out}_p$ and $\text{out}_n$ nodes experience voltage drops from the power supply. The speed of the voltage drop is determined by the input voltage of the comparator. Because of the positive latch in the comparator, the regenerative process begins to speed up the comparator decision.

The comparator output drives the SR latch in Fig. 17. The SR latch stores the comparison result during the pull-up phase of the comparator, and controls the feedback DAC timing. The $F1, N1$, and their respective inverting signals control the feedback signal as shown in Fig. 18. They drive the switches that connect either the positive supply voltage or ground as the 1-bit DAC feedback voltage. The timing is synchronized with $\Phi_2$ for the integrator operation. The Digit_N and Digit_P signals are connected to the digital output pads, which generate the modulator output captured by the logic analyzer for further analysis.

| TABLE IV |
| Performance Summary |
| Supply voltage | 0.9 V |
| Analog power consumption | 55 $\mu$W |
| Digital power consumption | 5 $\mu$W |
| Peak SNR | 82.2 dB |
| Peak SNDR | 73.1 dB |
| Dynamic range | 83 dB |
| Sampling frequency | 2 MHz |
| Signal bandwidth | 20 kHz |
| Oversampling ratio | 50 |
| Core size | 0.42 mm$^2$ |
| Figure of merit | 168 |
C. Complete Modulator Circuit

The complete modulator circuit is shown in Fig. 18. It has four integrators with a comparator and a latch. We have used two kinds of common-mode voltages. The input common-mode voltage is set to 0.3 V while the output common-mode voltage is set to the middle of the power supply voltage. The input common-mode voltage is lowered to give the OTA input differential pair sufficient voltage operating room.

The power supply rails, V_DD and ground, are used as the feedback reference voltages +V_ref and -V_ref. Two separate reference voltage pins with 10-μF and 0.1-μF decoupling capacitors are used to suppress noise interference [13].

The capacitor values are summarized in Table III. The capacitor value of the first integrator is chosen to satisfy the KT/C noise requirement as shown below [13]

\[
C_n = \frac{8KT(DR)}{V_{DD}^2M} \tag{6}
\]

where T is the absolute temperature, DR is the dynamic range, M is the oversampling ratio, and V_DD is used as the amplitude of a full-scale sinusoidal input. The oversampling ratio M is 50 in our design, and the DR is set to 95 dB for a design margin. For the power supply V_DD of 0.9 V, the required capacitance is calculated as 2.6 pF. With the extra noise margin, the final sampling capacitance is selected as 3 pF. The other capacitors are selected to satisfy the modulator coefficients in Table I. The second and the fourth integrators have small sampling capacitors, as shown in Table III. The third integrator has another input path, which is the local resonator with a coefficient value of only 1/36. In order to implement this small ratio, the size of the resonator capacitor is chosen to be 0.06 pF and the integrating capacitor as 2.16 pF.

Then, the third sampling capacitor is decided as 0.96 pF for the integrator gain of 0.44. If we try to reduce the sampling capacitor further, the resonator capacitor becomes too small, so the sampling and integrating capacitors of the third integrator look larger than those of the second and the fourth integrators.

### IV. Measurement Results

The designed modulator was implemented in a 0.13-μm standard CMOS process, and the fabricated chip is shown in Fig. 19. The threshold voltages of the pMOS and nMOS transistors are −150 and 200 mV, respectively. The die photo shows four operational amplifiers with their respective sampling and integrating capacitors on the top and bottom sides of the amplifier.

Capacitors are laid out in symmetry to match the signal path of the positive and negative inputs and outputs of the fully differential circuit. The capacitors in the first integrator are laid out with 750-fF unit capacitors. The second and fourth integrators have 50-fF unit capacitors, and the third one has 60-fF unit capacitors. The level shifters and output buffers are shown on the right side of the floor plan. They are used to interface with 3-V logics on the test board.

The output spectrums of the modulator with 16 k samples are shown in Figs. 20 and 21 with 8.667-kHz sinusoidal inputs. The noise floor is increased than in the behavioral simulation, which shows that more nonidealities such as the component mismatches and the power line noise are included in the circuit operation and measurements. As the amplitude of the input signal becomes higher, harmonic distortions appear in the spectrum.

The measured SNR and SNDR curves are shown in Fig. 22, with the input amplitude normalized by the reference voltage. The peak SNR and SNDR reach 82.2 dB and 73.1 dB, respectively. The dynamic range is measured as 83 dB with power consumption of 60 μW. The measurement results are summarized in Table IV.

The performance of our modulator is compared with other state-of-the-art sub-1-V modulators in Table V. To compare performances, the common FOM equation [14] is used, which is shown below.

\[
FOM = DR_{\text{ref}} \times 10\log \left( \frac{BW}{P} \right). \tag{7}
\]

The presented modulator shows the highest FOM among the modulators. The high FOM can be explained by several reasons. The low-voltage swings of the modulator caused by the feedforward architecture make the OTA circuits very power-efficient. With very low output swing, low-quesitient current OTA is designed without concern for slewing. Another reason comes from the simplicity of our circuit components. Our design does not include charge pumps, switched-op amps, or switched-RC integrators, which may require extra control circuits and extra current.

### V. Conclusion

A very low-power delta-sigma modulator is implemented in a 0.13-μm CMOS process. Input feedforward modulator architecture is used to reduce the voltage swings of the integrators. By reducing the integrator swings, more power-efficient OTAs can be used for low-power circuit design. The issues of parasitic integrator and switch leakage current are discussed. The circuit components are carefully laid out to minimize noise interference. The measurement results show that this modulator can be used for very low-power audio and sensor applications. The FOM comparison among the sub-1-V modulators proves that the presented modulator has highly optimized performance.

### REFERENCES

transistors by analog T-switch (A T-switch) and super cut-off
oversampled delta-sigma converters and power management circuits.
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a Senior Analog Designer for delta-sigma data converters. In 2001, he joined
[16] R. Gregorian
with 80 dB SNDR and 83 dB DR using a single-phase technique,” in 
IEEE ISSCC Dig. Tech. Papers, 2000, pp. 74–75.
[6] K.-P. Pun, S. Chatterjee, and P. R. Kinget, “A 0.5-V 74-dB SNDR
25-kHz continuous-time delta-sigma modulator with a return-to-open
ulator with 88-dB dynamic range using local switch bootstrapping,” 
sigma-delta modulator in 90-nm CMOS,” IEEE J. Solid-State Circuits, 
“A 114-dB 68-mW chopper-stabilized stereo multibit audio ADC in
[12] A. Gharbiya and D. A. Johns, “On the implementation of input-feed-
[14] T. Schreier and G. C. Temes, Understanding Delta-Sigma Data Con-
order SC ladder filter in 0.35-μm CMOS technology,” IEEE Trans.
current mechanisms and leakage reduction techniques in deep-submi-
2003.
[19] K. Ishida, K. Kanda, A. Tantrakarn, H. Kawaguchi, and T. Sakurai,
“Managing subthreshold leakage in charge-based analog circuits with low-
Isub transistors by analog T-switch (A T-switch) and super cut-off
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